QSFP+ Copper Cable Assembly

Overview

QSFP+ (Quad Small Form-factor Pluggable Plus) copper direct-attach cables are suitable for very short distances and offer a highly cost-effective way to establish a 40-Gigabit link between QSFP+ ports of QSFP+ switches within racks and across adjacent racks. These cables are used for 40GbE and Infniband standards, to maximize performance. QSFP+ are designed to meet emerging data center and high performance computing application needs for a high density cabling interconnect system capable of delivering an aggregate data bandwidth of 40Gb/s. This interconnect system is fully compliant with existing industry standard specifications such as the QSFP MSA and IBTA (InfiniBand Trade Association). The QSFP+ cables support the bandwidth transmission requirements as defined by IEEE 802.3ba (40 Gb/s) and Infiniband QDR (4x10 Gb/s per channel) specifications.

Features

- Compliant QSFP MSA specifications
- Fully compatible with IEEE802.3ba and Infiniband QDR specifications
- 40 Gb/s total bandwidth
- 4 independent duplex channels operating at 10Gbps, also support for 2.5Gbps, 5Gbps data rates
- 100 ohm differential impedance system
- Single 3.3V power supply, low power consumption, <1.5W
- Low Near-End Crosstalk(NEXT)
- Operating case temperature: -40 to 85°C
- All-metal housing for superior EMI performance
- Precision process control for minimization of pair-to-pair skew
- AC coupling of PECL signals
- EEPROM for cable signature & system communications
- 30 AWG to 24 AWG cable sizes available
- RoHS compliant

Applications

► Data

Servers
Networked storage systems
Routers
External storage systems
Data Center networking

► Communications

Switches
Routers

► Industry Standards

InfiniBand Trade Association (IBTA)
IEEE802.3ba
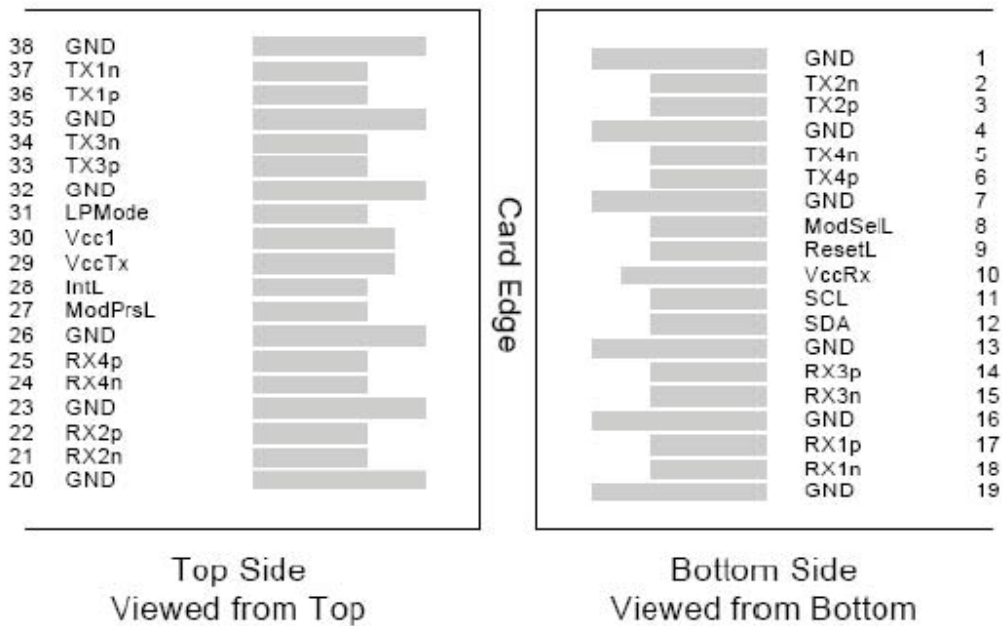40Gigabit Ethernet (40G BASE – CR4)

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	125	degC	
Relative Humidity (non-condensation)	RS	-	85	%	
Operating Case Temperature	Topc	-40	85	degC	1
Supply Voltage	VCC3	-0.3	3.6	V	
Voltage on LVTTL Input	Vilvttl	-0.3	VCC3　+0.2	V	

NOTE: Stress or conditions exceed the above range may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not applied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	Topc	-40	85	degC
Relative Humidity (non-condensation)	RS	-	85	%
Supply Voltage	VCC3	3.135	3.465	V
Power Supply Currenct	ICC3	750	-	mA
Total Power Consumption	Pd	-	2.0	W

Pin Assignments and Descriptions

```
38  GND                              GND    1
37  TX1n                             TX2n   2
36  TX1p                             TX2p   3
35  GND                              GND    4
34  TX3n                             TX4n   5
33  TX3p                             TX4p   6
32  GND                              GND    7
31  LPMode                           ModSelL 8
30  Vcc1                             ResetL 9
29  VccTx                            VccRx  10
28  IntL                             SCL    11
27  ModPrsL                          SDA    12
26  GND                              GND    13
25  RX4p                             RX3p   14
24  RX4n                             RX3n   15
23  GND                              GND    16
22  RX2p                             RX1p   17
21  RX2n                             RX1n   18
20  GND                              GND    19
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Card Edge

Top Side
Viewed from Top

Bottom Side
Viewed from Bottom

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1

5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		Vcc Rx	+ 3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CMLO	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CMLO	Rx1p	Receiver Non-Inverted Data Output	
18	CMLO	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CMLO	Rx2n	Receiver Inverted Data Output	
22	CMLO	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CMLO	Rx4n	Receiver Inverted Data Output	1
25	CMLO	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTLO	ModPrsL	Module Present	
28	LVTTLO	IntL	Interrupt	
29		Vcc Tx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTLI	LPMode	Low Power Mode	
32		GND	Ground	1

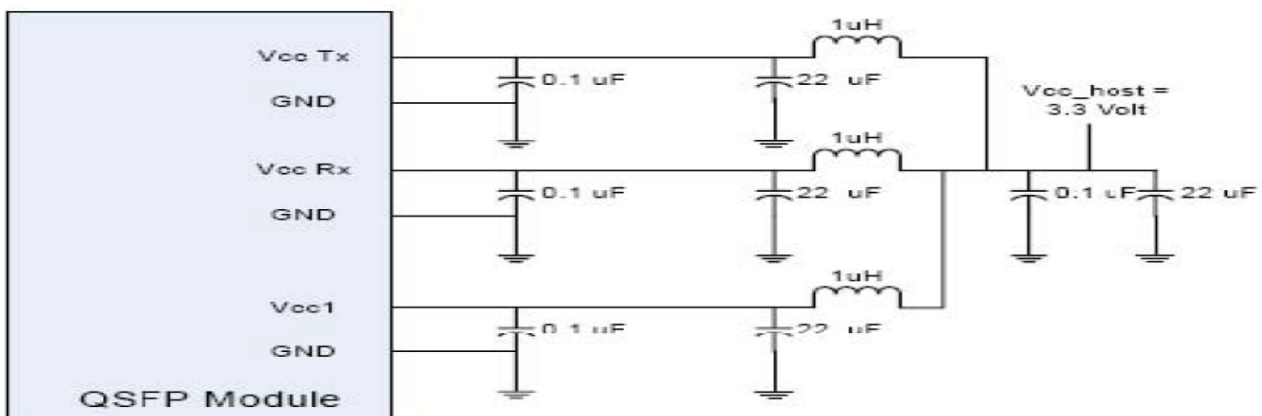| 33	CMLI	Tx3p	Transmitter Non-Inverted Data Input	
34	CMLI	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CMLI	Tx1p	Transmitter Non-Inverted Data Input	
37	CMLI	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

1. GND is the symbol for signal and supply (power) common for QSFP modules. All are common within the QSFP module and all module voltages are referenced to this potential otherwise noted. Connect these directly to the host board signal common ground plane.

2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Recommended power supply filtering Example of QSFP Host board schematics.

A typical host board mechanical layout for attaching the QSFP transceiver is presented below. The recommended host electrical connector should be a 38-pin IPASS right angle connector assembly (example: Tyco PN: 1761987-9) and the cage assembly should be QSFP single cage (example: Tyco PN: 1888617-1).

Recommended PCB layout

A typical host board mechanical layout for attaching the QSFP transceiver is presented below. The recommended host electrical connector should be a 38-pin IPASS right angle connector assembly (example: Tyco PN: 1761987-9) and the cage assembly should be QSFP single cage (example: Tyco PN: 1888617-1).
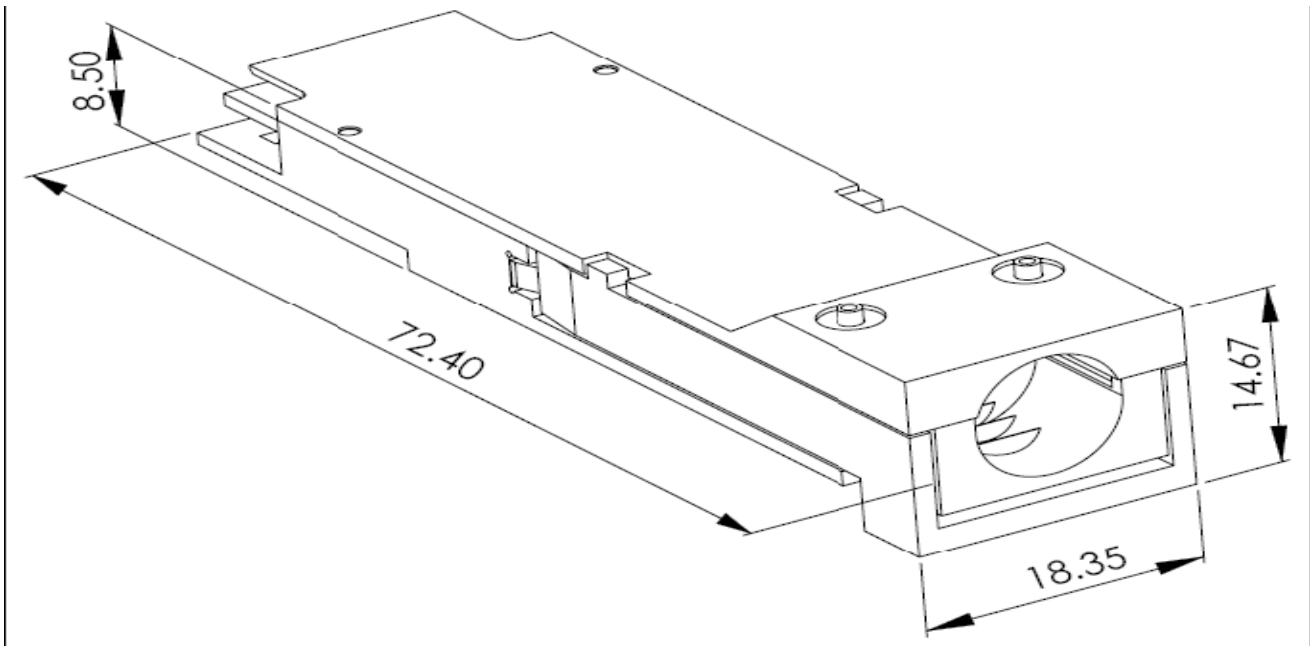
Top drawing labels:

- BSC
- ℄ OF -K- & -L-
- 10.6
- 11.3 MIN
- -X-
- -Y-
- BSC
- Ø1.05±0.05
- ⊕ Ø0.10Ⓜ A KⓈ LⓈ
- 12 PLC
- 9 6 PLC
- 7.6
- 3.1
- -L-
- SEE DETAIL A
- 3.4
- 7.2
- 16.8
- 19
- 17.9 REF
- 22.15 MIN
- -C-
- 1.1
- 7.6
- -K-
- 3.1
- 37 MAX
- CROSS-HATCHED AREA DENOTES COMPONENT AND TRACE KEEP-OUT (EXCEPT CHASSIS GROUND)
- THIS AREA DENOTES COMPONENT KEEP-OUT (TRACES ALLOWED)

△1 DATUM -X- AND -Y- ESTABLISHED BY CUSTOMER'S FIDUCIAL
△2 DATUM -A- IS TOP SURFACE OF HOST BOARD.
△3 LOCATION OF EDGE OF PCB IS APPLICATION SPECIFIC.
△4 FINISHED HOLE SIZE.

Bottom drawing labels:

- ℄ OF -K- & -L-
- Ø1.55±0.05
- ⊕ Ø0.05 A X KⓈ -L-
- 5.18
- 2.5
- 1.8±0.03
- ⊕ 0.05Ⓜ KⓈ LⓈ
- 38 PLC
- 1 38
- 15.02 MAX
- 19.2 MAX
- 15.80
- 19.2 MAX
- ℄ OF -C-
- 0.35±0.03
- ⊕ 0.05Ⓜ KⓈ LⓈ
- 38 PLC
- 0.8 36 PLC
- 19 20
- 0.4
- Ø1.55±0.05
- ⊕ Ø0.05 A X Y -K-
- 1.69 MAX
- 3.05 MIN
- 10.3 MAX

△1 CENTERLINE OF PAD.
△2 SURFACE TRACES PERMITTED WITHIN THIS LENGTH.
△3 INDICATED HOLES ARE OPTIONAL.

6

QSFP Copper Module Outline for System Design

8.50

72.40

14.67

18.35

Mechanical Dimensions

19   20

1   38

L

W

X1

38   1

20   19

X2