VS1797SM

Product Specification
NFC Module
Ver.: 2.1

Document Release	data	Modification	Initials	Approved
Version 1.0	2017/3/17	Initial Version		
Version 2.1	2017/4/10	Latest Version		

1.General Description

VS1797SM is based on the Broadcom® BCM20797SM2 chip design, highly integrated, low-power, low-cost, 40 nm NFC controller .The BCM20797SM2 is the third-generation NFC Controller from Broadcom. The size of the NFC module is 12.7*12.0*1.6MM,20-pin design.

2.FEATURES

NFC

• Support for:

– ISO/IEC 18092

– ISO/IEC 21481

– ISO/IEC 14443 Type A, Type B, and Generic B Prime cards (CE mode only for B Prime cards)

– Japanese Industrial Standard (JIS) (X) 6319-4

– ISO/IEC 15693 standards.

– Extended data rates up to 848 kbps for all

NFC modes, including P2P

• ARM Cortex-M3 with 256 KB of ROM and 96 KB of SRAM

• Host interface options:I2C-compatible (3.4 Mbps max.)

•Reader/Writer (R/W) mode:

– MIFARE Reader to read/write MIFARE Classic encrypted tags and cards

– 5V TX driver capable of delivering up to 1W of power to provide support for smaller antenna form factors

– Sensitive reader demodulator for extended range operation and low frame-error rates

– Support for Fast Tag Read (FTR) mode

APPLICATIONS

• Contactless payment

• Mobile handsets

• Simplified connectivity between wireless devices

• Contactless ticketing

• Peer-to-peer mode transactions

• Smart-poster tag reading/writing

3.Host Interface---I2C

The main features of the VS1797S I2C host interface include the following:

• Slave mode.

• Low-speed mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps) supported. Due to practical constraints imposed by parasitic capacitance and pull-up resistor values, especially in a multidrop system, Broadcom engineers recommend that this be limited to 1.7 Mbps.

• The following automatically detected addresses are supported: 0x77, 0x76, 0x66, and 0x1FA.

– Detection of whether an address is 7 bits or 10 bits is automatic.

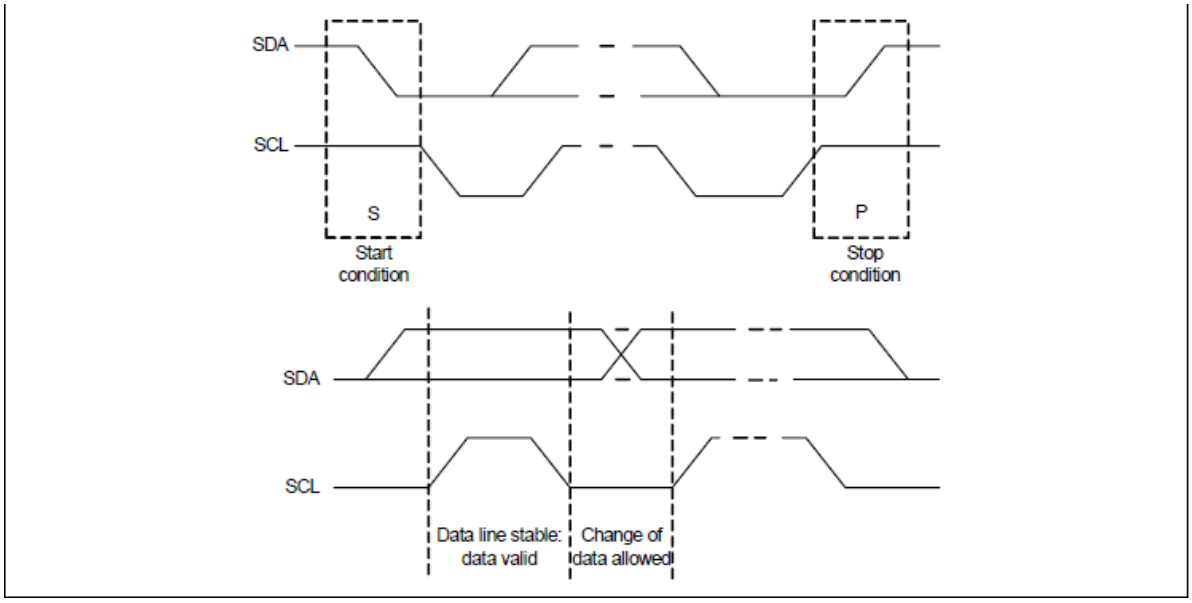
– The address detected in the first message sent to the device after power-up is the address used for the current power cycle, and the other addresses are subsequently masked out. However, after the boot-up, subsequent commands can be sent to change the address for the remainder of the power cycle.

• Dedicated TX and RX FIFOs are 271 bytes each.

• A digital deglitching filter is implemented. It uses a simple majority of three and filters spikes of up to 40 ns.

• A high-speed reference clock is not required for operation. Defined accesses in the SR mode initiate the wake-up function.

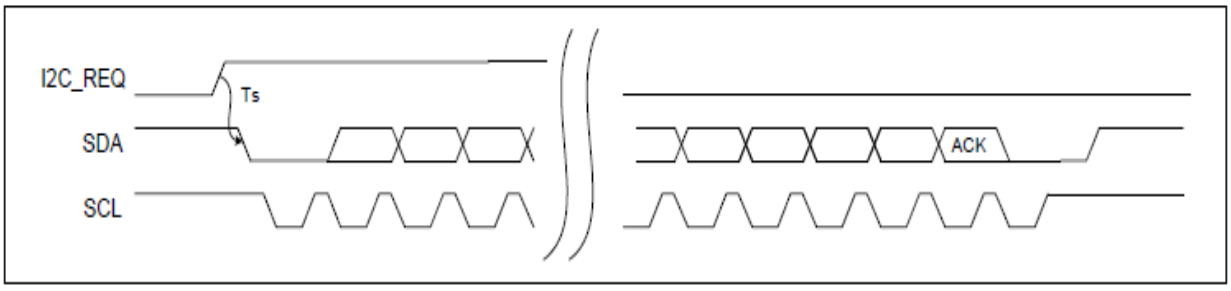
I2C Timing Waveform



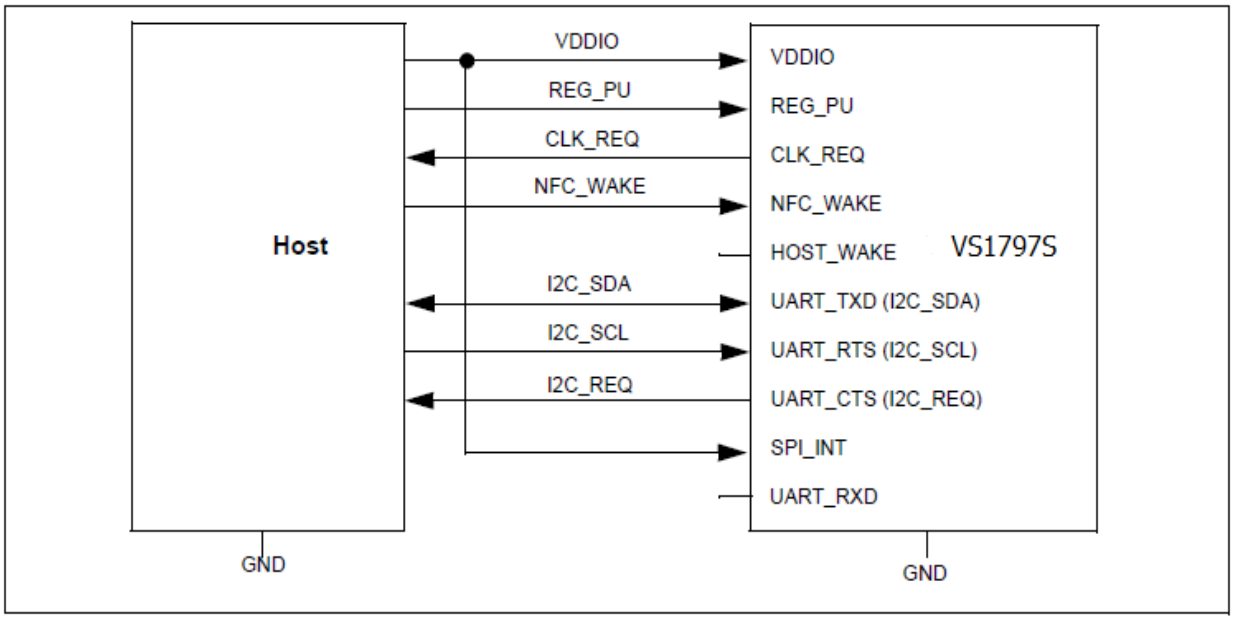
I2C_REQ is an output signal from the BCM20797SM2 to the host to indicate that the BCM20797SM2 is going to communicate.

The I2C_REQ signal stays high until after the first byte has been read by the host.

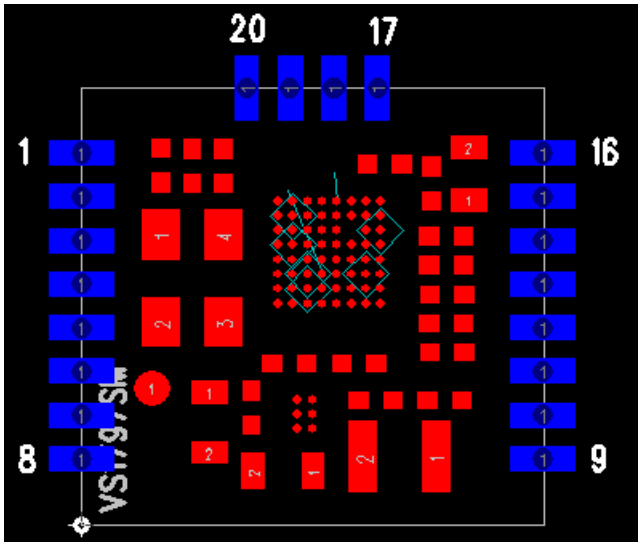
I2C_REQ Timing Waveform



I2C Host Interface



4.Pin Information <TOP VIEW>



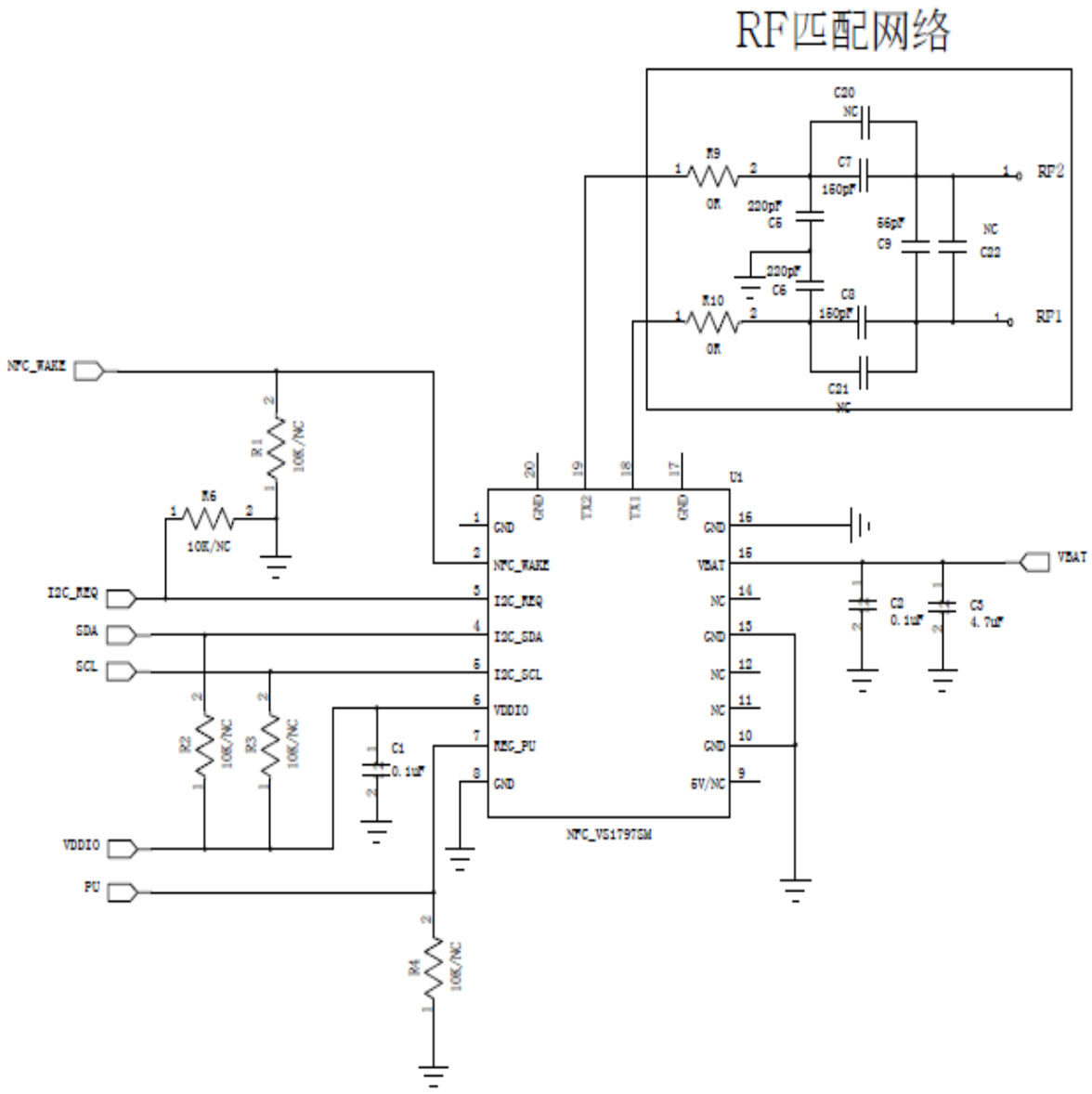
PIN NUMBER	Device Pin Name	*I/O*	Polarity	Description
1	GND	—		System ground
2	NFC_WAKE	I	Active high	NFC wake-up. If the BCM20797SM2 is asleep, pulling NFC_WAKE high will wake it up. When this pin is held high, the SR mode cannot be enabled. When NFC_WAKE is pulled low, the BCM20797SM2 can subsequently enter the SR mode when it is inactive. The default is an internal 40–50 kΩ pull-down at power-up. After the SR mode is enabled (when the host sends the sleep enable command), the pulldown is disabled (that is, no pull-up or pull-down).
3	I2C_REQ	O	Active high	BSC Request. Signal from the VS1797S to the host that the VS1797S is going to communicate with.
4	I2C_SDA	I/O	—	BSC Serial Data Line. Bidirectional serial data between the host and the VS1795P1.
5	I2C_SCL	I	—	BSC Serial Clock. Generated by the host to the VS1795P1.
6	VDDIO	P	—	I/O supply; externally regulated
7	REG_PU	I	Active high	Regulator power-up. Low: Shut down with all LDOs off. High: LDOs are available. Internal 4MΩ pull-down resistor. Once asserted, the host GPIO line used for REG_PU

				should be glitch-free and must not be toggled after a power-up has started.
8	GND			System ground
9	5V/NC	I	Default NC	External 5V input PIN，Default is NC.
10	GND			System ground
11	VDDSWP_IN0			Platform UICC supply in to power switches for SWP-0 & SWP-1
12	VDDSWP_O			Supply out to UICC/secure element on SWP-0
13	GND			System ground
14	SWPIO_0			SWP I/O for UICC/Secure Element on SWP-0
15	VBAT			Battery/Power supply in
16	GND			System ground
17	GND			System ground
18	ANTRDR_P			Antenna Reader/Tag positive phase
19	ANTRDR_N			Antenna Reader/Tag negative phase
20	GND			System ground

5.Typical circuit and pin instructions

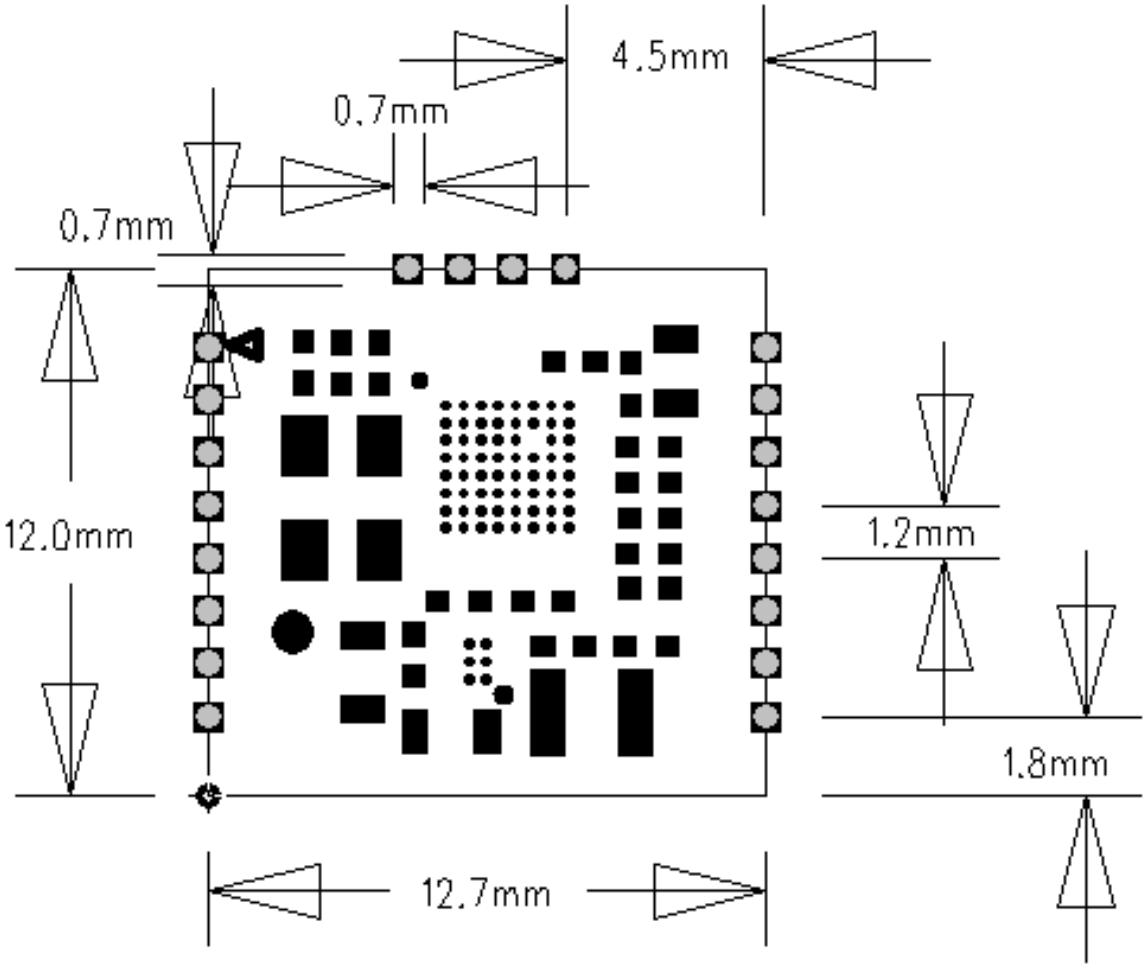
Note: VBAT 电压范围（2.7V-5V），VDDIO 电压范围（1.6V-3.5V）

Recommend：VBAT 3.3V；VDDIO 3.3v 或 1.8V；



<详见设计指导>

6.Package Information



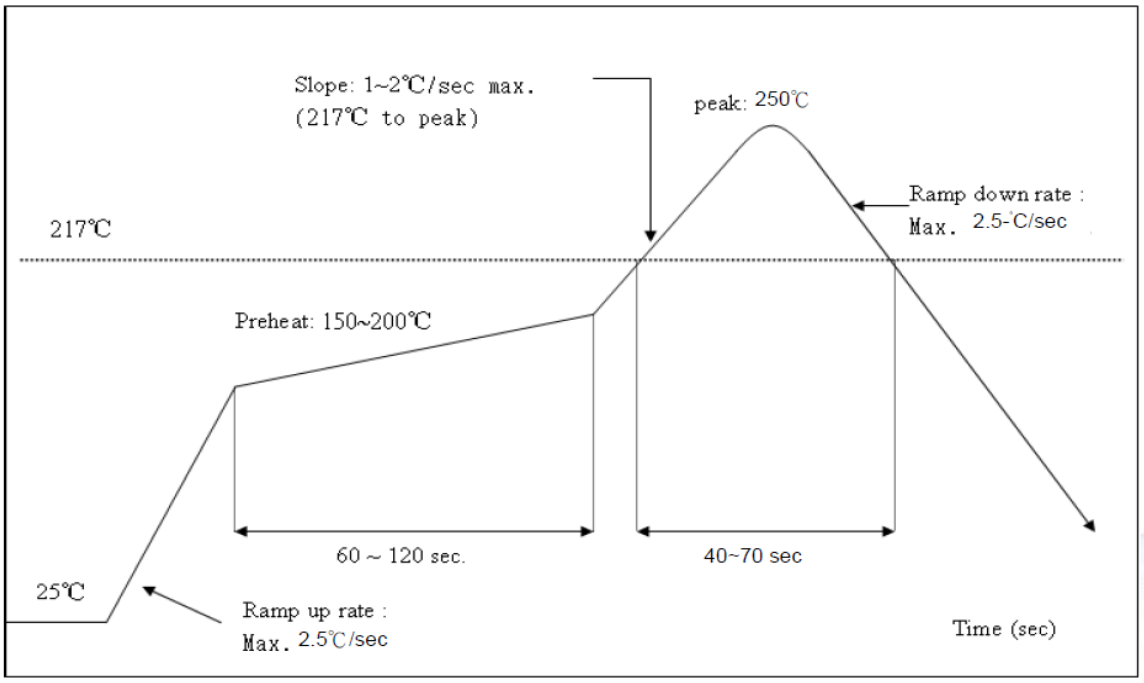
TOP VIEW

◎SMT 规范：

Referred to IPC/JEDEC standard.
Peak Temperature : <250℃
Number of Times : ≤2 times

SMT reflow profile 参数值

需使用氮气N2,含氧量建议为1500+/-500 ppm



2. Peak package body temperature: 225℃ ☐ 240℃ ☐ 250℃ ☑ 260℃ ☐

=> 如规格书中所说明，模块在制程中最高温度不超过250度C

5. If baking is required, devices may be baked for 24 hours at 125±5℃

1.模块制造厂出货前置作业:测试过模块良品经24小时烘烤后 真空包装出货，则整卷未拆封不需经过烘烤可直接上件贴片。

2.如规格书中所说明，整卷包装已拆封未贴片完之剩下的模块余数，因暴露于空气中可能已接触空气中的水气，故于下次上件贴片前就须先进入烤箱烘烤，烘烤条件24小时125度C。

注意：烘烤时，须考虑包装材料的最高耐受温度！

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