ALLDAQ
Competence in Measurement

Manual

Rev. 1.0 EN

ADQ-330/340 series

Isolated Multi I/O board – up to 32 analog inputs, 4 analog outputs, 32 digital I/Os, counter …

Imprint

Manual ADQ-330/340 series
Rev. 1.0
Date: 04/19/2018

Manufacturer and Support

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1. Introduction

Please check the box and the content for damages and completeness before taking the device into operation. If any fault should be detected please inform us immediately.

- Shows the packing some evidence to damaging during transport?
- Any traces of use to be recognized at the device?

The device may not be taken into operation if it is damaged. In case of doubt please contact our technical service department.

Please read – before installing the device – this manual watchfully!

1.1 Scope of delivery

- ALLDAQ board of the ADQ-330/340 series for CompactPCI (4 HP) or PCI-Express
- Additional mounting bracket/bezel with 25-pin D-Sub female connector to 20-pin IDC connector for cPCI systems (ADQ-AP-D25F-cPCI) resp. PCI-Express slots (ADQ-AP-D25F-PCI)
- 25-pin D-Sub male connector
- 3-pin mating plug for ST1, Phoenix type MC 1,5/ 3-ST-3,5
- Driver software and documentation under: www.alldaq.com/en/downloads

Optional:

- Special terminal block for ADQ-330/340 series (ADQ-TB-300-HUT)
- 2 x 68-pin VHDCI cable (male - male), double-shielded, twisted-pair wires, length: 1.2 m (ADQ-CR-VHDCI-68M/68M-1,2m), art. no.: 150597 (2 x)
- 2 x 68-pin VHDCI cable (male - male), double-shielded, twisted-pair wires, length: 1.8 m (ADQ-CR-VHDCI-68M/68M-1,8m), art. no.: 146813 (2 x)
- HDMI cable, length: 1 m (ADQ-CR-HDMI-MM-1m), art. no.: 127015

1.2 Safety instructions

Necessarily note the following advices:

- Necessarily avoid touching of cables and connectors inside the PC with the board.
- Never expose the device to direct solar radiation during operation.
- Never run the device near heat sources.
- Protect the device before humidity, dust, liquids and fumes.
- Don´t use the device in damp rooms and never in explosive areas.
- A repair may only be done by trained and authorized persons.

- Please note before initial operation of the device especially when using voltages greater 42 V the installation rules and all relevant standards (including VDE standards).
- We recommend to tie all unused inputs basically to the corresponding reference ground to avoid cross talk between the input lines.
- Before connecting or removing cables with your board always disconnect your field wiring from the power supply.

- Ensure that no static discharge can occur passing the board when handling it. Follow the standard ESD safety precautions (see also chapter 2.1 on page 19).
- Never connect devices with voltage-carrying parts, especially not with mains voltage.
- The user must take appropriate precautions to avoid unforseeable misuse.

For damages caused by improper use and subsequent damages any liability by ALLNET® GmbH Computersysteme is excluded.

1.3 Location of installation and mounting

The CompactPCI resp. PCI-Express boards of the ADQ-330/340 series are multi I/O data acquisition boards for industrial use. Depending on the model they are for installation…

… into a free PCI-Express slot (ADQ-330/340-PCIe), or

… into a free CompactPCI slot (ADQ-330/340-cPCI).

PC boards may not be taken into operation outside of appropriate PC systems. For the order of operation on installing the devices please read the chapter „Initial operation" in this manual and the documentation of your PC.

The ADQ-330/340 series may only be used in dry rooms. PC boards are not for use with tough environment conditions (e.g. outside). Ensure a very good ventilation. Take care for proper fitting of the connection cables. Installation has to be done in a way that the cables (PC connection and field wiring) are not in tension else they could release itself.

1.4 Short description

The ALLDAQ multi I/O boards of the ADQ-330/340 series are available isolated (ADQ-34x) and non-isolated (ADQ-33x) versions for CompactPCI bus. They offer a very wide functional scope for universal use in the industrial field. For extra fail-safe measurements on the ADQ-34x models the analog and digital functional groups are electrically isolated from each other and PC ground.

Common to all models is the simultanous 18 bit analog input section with 16 or 32 differential input channels which are aggregated in channel groups (also called AI ports) with 8 channels each. Depending on the number of actively used channels per AI port the sample rate is between 200 kS/s and 800 kS/s. The values can be sampled as single values or timer-controlled. On demand the measurement can be started by one external trigger input per AI port. The input ranges ±10.24 V, ±5.12 V, 0-10.24 V, 0-5.12 V insure always the best accuracy with full 18 bit resolution. On request a 0-20 mA input range is possible.

The 16 bit analog output section with up to 4 channels can output single values or timer-controlled with up to 500 kS/s per channel. Beside the standard signal curves like sine, rectangular, triangular, ramp and other pre-defined signals the boards can also generate arbitrary waveforms, e. g. for hardware in the loop (HiL) applications.

The boards of the non-isolated ADQ-33x models are equipped with 32 TTL digital-I/Os whose direction can be switched by port (8 bit wide). The ADQ-34x models offer 16 TTL digital-I/Os, 8 isolated digital inputs (up to 35 V) and 8 isolated digital outputs with power drivers up to 600 mA per output. The voltage level of all TTL digital I/Os can be switched between +3.3 V and +5 V in common by software.

As far as a digital port is configured as input, the input lines can be monitored on bit-change and generate an interrupt. The streaming operation enables the continuous reading resp. writing of a bit-pattern from resp. to all DI, DO and DIO ports up to 10 kHz (depending on the operating system and computer configuration).

The analog and digital I/Os of the board are divided to two 68-pin VHDCI female connectors, the 16 TTL digital I/Os are available on demand by an additional mounting bracket/bezel (included). A 3-pin Phoenix type clamp provides power for your external wiring with short-circuit-proof 5 V / 3 A and 12 V / 2 A from the PC. Both voltages are fused by a resetable fuse of type Polyfuse.

Special functions* like 32 bit counter, I^2C bus, incremental encoder, frequency measurement and PWM output are available by a HDMI connector (in preparation).

- 32 bit counter, clock source internal or external up to 66 MHz (inputs: enable, ext. trigger, ext. clock, output: strobe)
- I^2C bus port, operation of the ADQ-330/340 as master in fast mode (clock: SCL, data: SDA)
- Incremental encoder port (A input, B input, ext. reset input)
- Frequency measurement input for rectangular signals up to 660 kHz (counter input)
- PWM output of a rectangular signal up to 33 MHz with adjustable duty factor (enable input, PWM output)

The voltage level of all special I/Os can be switched between +3.3 V and +5 V by software in common with the TTL digital I/Os.

1.4.1 The ADQ-330 series in overview

	ADQ-331 (Art. no. 142251)	ADQ-332 (Art. no. 142252)	ADQ-334 (Art. no. 142253)
PC interface	CompactPCI		
Analog inputs			
Number of channels	16 pseudo-differential		32 pseudo-differential
Resolution	18 bit		18 bit
Sample rate	200 kS/s up to 800 kS/s synchronous (1 channel: 800 kS/s, 2 channels: 550 kS/s, 8 channels: 200 kS/s)*		
Input ranges	±10.24 V, ±5.12 V, 0..10.24 V, 0..5.12 V (0..20 mA on request)		
Isolation AI section	see ADQ-340 series (table)		
Analog outputs			
Number of channels	–	2 channels	4 channels
Resolution	–	16 bit (±10.24 V)	
Output rate	–	500 kS/s synchronous	
Isolation AO section	see ADQ-340 series (table)		
Digital I/Os			
TTL I/Os	32 TTL DIOs (3.3 V or 5 V switchable)		
Isolated DIOs	see ADQ-340 series (table)		
Special functions**	1 x 32 bit counter, 1 x I^2C bus, 1 x incremental encoder, 1 x frequency measurement, 1 x PWM output		

Table 1: Overview ADQ-330 series

*Sample rate depending from number of actively used channels per channel group (AI-Port), one channel group consists of 8 channels (1 channel: 800 kS/s, 2 channels: 550 kS/s, 8 channels: 200 kS/s)
**in preparation

1.4.2 The ADQ-340 series in overview

	ADQ-341 (Art. no. 142254)	ADQ-342 (Art. no. 142255)	ADQ-344 (Art. no. 142256)
PC interface	CompactPCI		
Analog inputs			
Number of channels	16 pseudo-differential		32 pseudo-differential
Resolution	18 bit		18 bit
Sample rate	200 kS/s up to 800 kS/s synchronous (1 channel: 800 kS/s, 2 channels: 550 kS/s, 8 channels: 200 kS/s)*		
Input ranges	±10.24 V, ±5.12 V, 0..10.24 V, 0..5.12 V (0..20 mA on request)		
Isolation AI section	1500 VDC (60 s) towards PC ground		
Analog outputs			
Number of channels	–	2 channels	4 channels
Resolution	–	16 bit (±10.24 V)	
Output rate	–	500 kS/s synchronous	
Isolation AO section	1500 VDC (60 s) towards PC ground		
Digital I/Os			
TTL I/Os	16 TTL DIOs (3.3 V or 5 V switchable)		
Isolated DIOs	8 isolated DIs, 8 isolated DOs up to 600 mA per output		
Isolation DIO section	500 VAC gegenüber PC-Masse		
Special functions**	1 x 32 bit counter, 1 x I^2C bus, 1 x incremental encoder, 1 x frequency measurement, 1 x PWM output		

Table 2: Overview ADQ-340 series

*Sample rate depending from number of actively used channels per channel group (AI-Port), one channel group consists of 8 channels (1 channel: 800 kS/s, 2 channels: 550 kS/s, 8 channels: 200 kS/s)
**in preparation

1.5 System requirements

1.5.1 Hardware

- PC system with a current Intel® or compatible processor based on the x86(-64) architecture
- A free PCI-Express x1 resp. CompactPCI slot with 4 HP width
- On demand one further PCI slot resp. CompactPCI slot (4 HP) for 16 TTL DIO ports

1.5.2 Software

- **Operating system**
  - Windows 7 (32 and 64 bit)
  - Windows 8/8.1 (32 and 64 bit)
  - Windows 10 (32 and 64 bit)

- **ALLDAQ device driver**
- **Some tools and examples require the Microsoft .NET framework.**

1.6 The ALLDAQ driver system

1.6.1 Architecture

The ALLDAQ driver system consists of several kernel mode device driver and an user mode DLL, which provides the application programming interface (API). The API is exported from a shared library for the different Windows platforms (32/64 bit). During installation, the libraries are copied to the respective Windows system directory.

A so-called "board" represents a hardware device which is installed in your computer and connected via PCI (Express) bus.

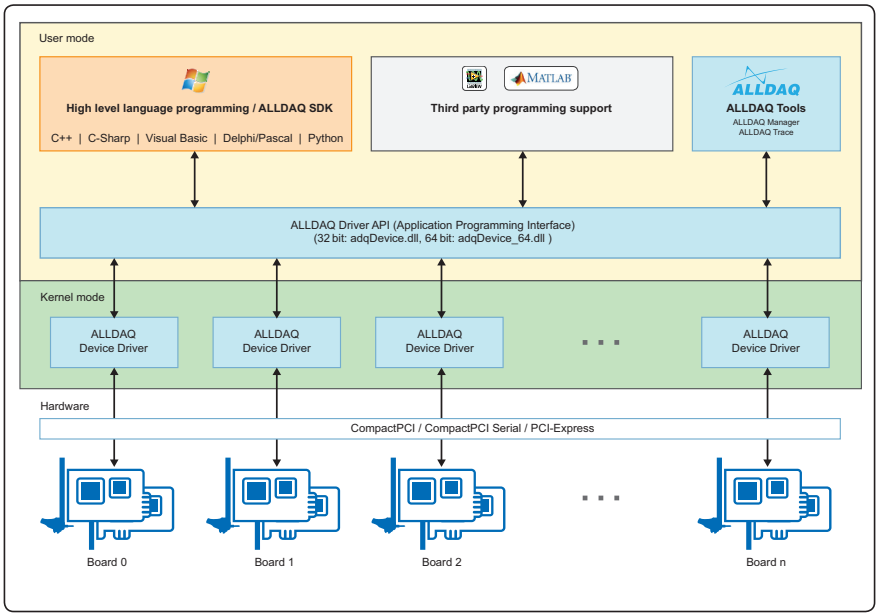


Figure 1: ALLDAQ driver system architecture

All boards are listed in the Windows Device Manager under "ALLDAQ Data Acquisition Devices". A board consists of one or more modules of a certain type, e. g. "Digital Input", "Digital Output", "Analog Input", "Counter" etc. Modules can always be used independently of each other. The board index is assigned by the operating system during the boot process.

1.6.2 ALLDAQ-Launcher

Using the so-called ALLDAQ Launcher you can conveniently access the ALLDAQ Manager, the Software Developer Kit (SDK), software tools, help files and manuals. You can open the ALLDAQ Launcher in the info area of the taskbar with the right mouse button or via the Windows start menu.

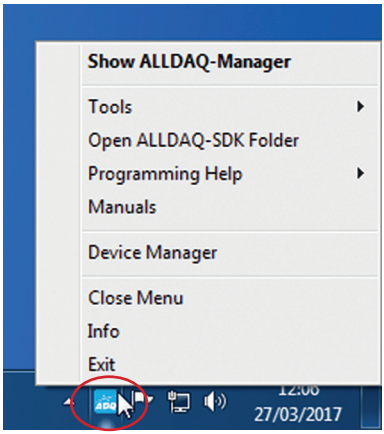


Figure 2: ALLDAQ-Launcher

1.6.3 ALLDAQ-Manager

The ALLDAQ-Manager gives you a quick overview of the installed ALLDAQ hardware and a central access to the software developer kit (SDK), software tools and help files. You can open the ALLDAQ Manager by the so-called ALLDAQ Launcher in the info area of the taskbar or via the Windows start menu.

Features in overview:

- Information on the installed ALLDAQ hardware in overview
- XML export of the driver configuration for archiving and support
- Tool for interactive illustration of the pin-assignment with the possibility to generate a PDF
- Tool for user calibration of analog modules
- Convenient access to the software developer kit (SDK) for high-level language programming with examples and simple test programs
- Quick access to the help files and hardware manuals

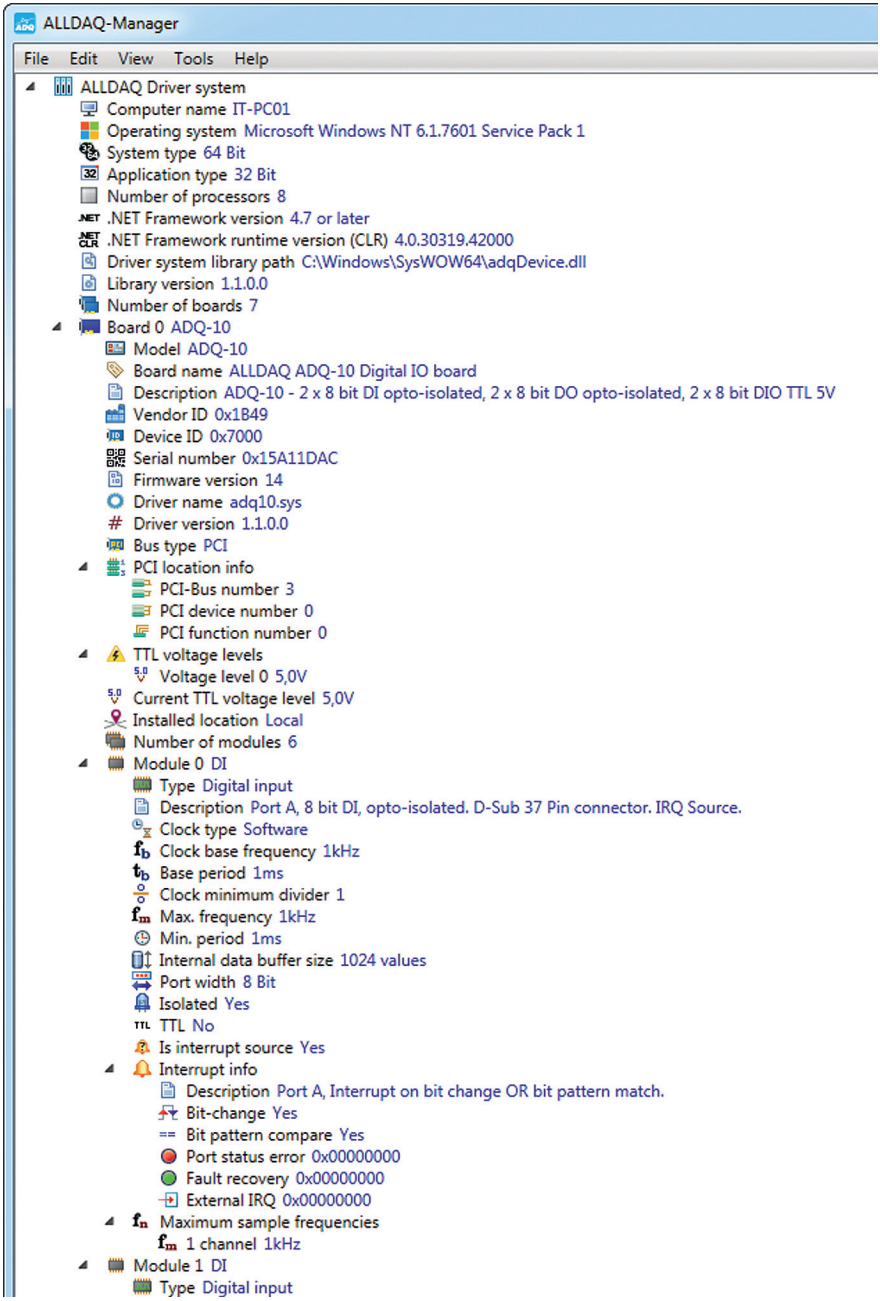


Figure 3: **ALLDAQ-Manager**

1.6.4 Pin-assignment tool

Tool for interactive illustration of the pin-assignment with the possibility to generate a PDF.

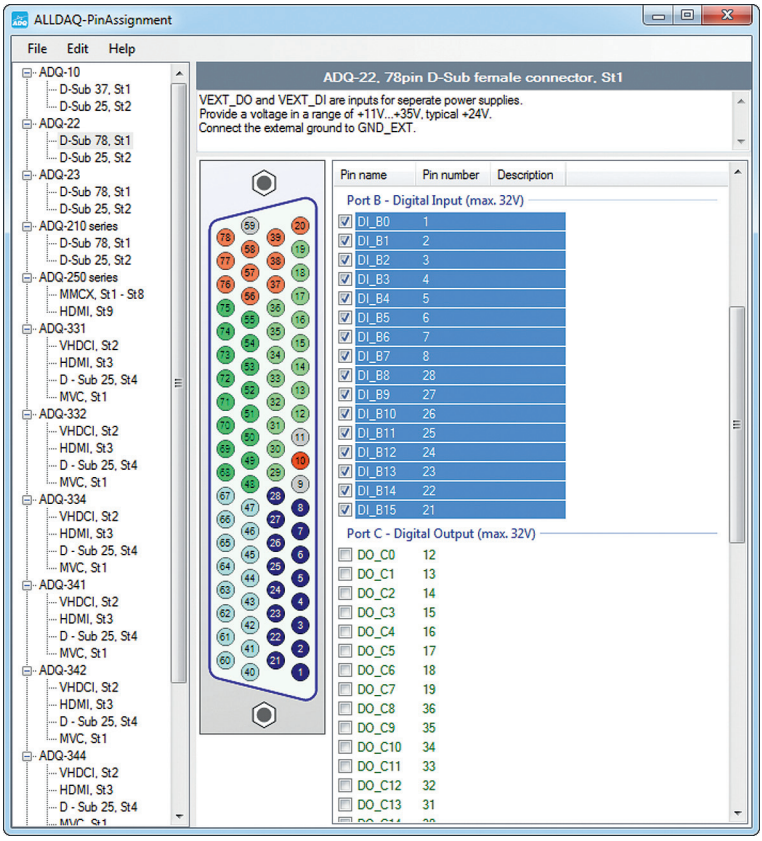


Figure 4: Pin-Assignment tool

1.6.5 Software developer kit (SDK)

The software developer kit (SDK) offers programming support with examples for C++, C#, Visual Basic, Delphi/Pascal and Python®. Numerous EXE programs can be used to test the individual function groups.

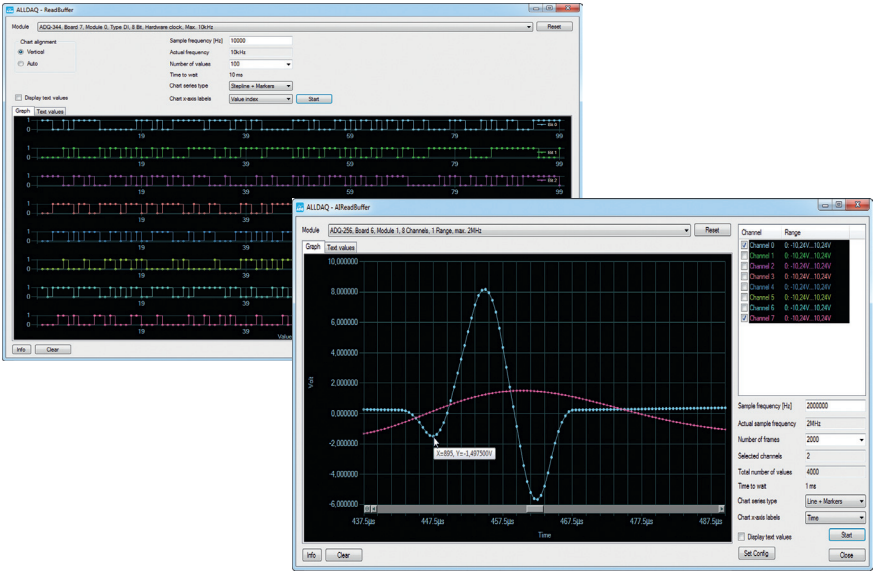


Figure 5: Example programs

1.6.6 Help files

Detailed help files for driver API, SDK, Matlab, LabVIEW and Python make programming easier.

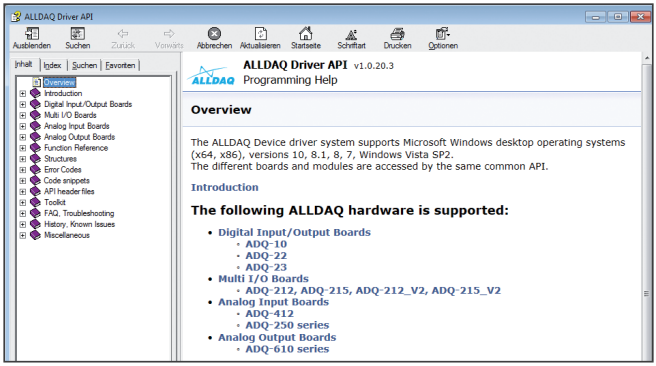


Figure 6: Help files for API, SDK, Matlab, LabVIEW and Python

1.6.7 LabVIEW™ support

A library with virtual instruments (VIs) for easy access to the ALLDAQ hardware is included with the ALLDAQ SDK.

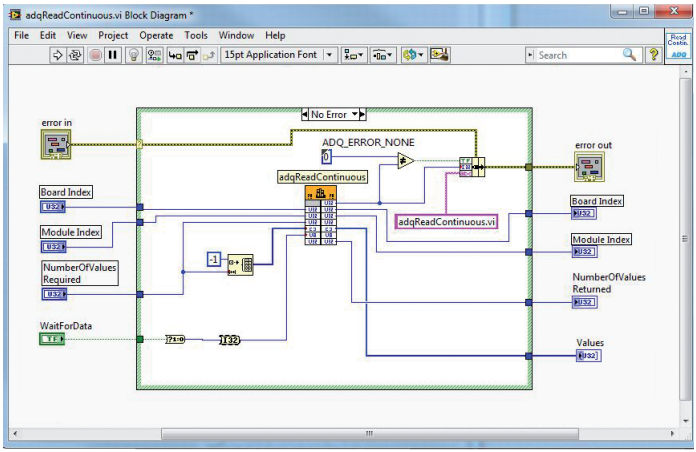


Figure 7: Graphical programming with LabVIEW™ VIs

1.6.8 MATLAB® support

An adapted MATLAB® interface for the ALLDAQ hardware with examples and a help file is included with the ALLDAQ SDK.

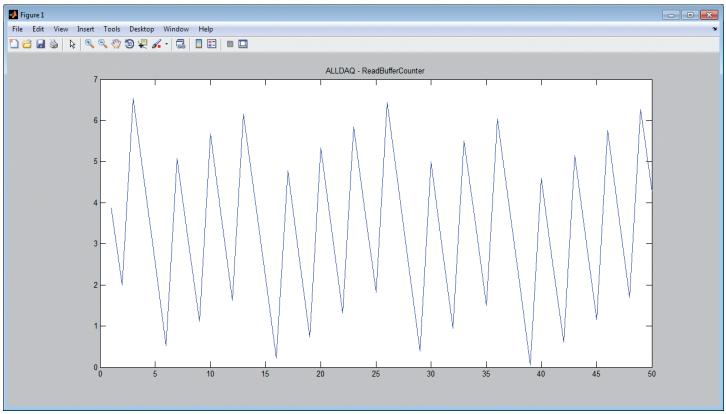


Figure 8: Simple visualisation of a signal in MATLAB®

2. Initial operation

2.1 Installing the board

Please read the manual of your computer prior installing the board regarding the installation of additional hardware components.

Handling the board should be done with care to ensure that the device will not be damaged by electrostatic discharge (ESD), mechanical stress or current surges. Ensure to take all safety precautions to avoid an electric shock and follow the standard ESD safety precautions.

Follow this order of operation:

- Unplug the mains plug of your PC system.
- Open the housing as described in the manual of your PC system.

- Make sure that electrostatic discharge cannot occur via the board when you plug it in. At least one hand should be grounded in order to dissipate any static charge.
- Only for PCI Express models: for the +5 V supply of the board an additional supply by the PC power supply is neccessary (current consumption without load 300 mA typ.). Connect a free power connector of your PC (e. g. as used for powering drives) with the appropriate „MOLEX" male connector of your PCIe board (see the following diagram). On demand adapter (cables), e. g. from 13-pin SATA power supply male connector to 4-pin MOLEX female connector are available in specialized shops.

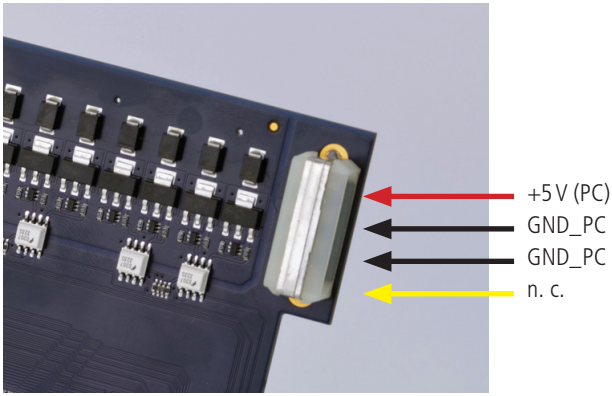


Figure 9: 5 V supply for PCI Express models

Attention: If you take the board into operation without connecting the +5 V supply the board can be irreverseable damaged!

- Push the plug-in board carefully and with only a little force into the appropriate slot. Check that the board is not cant and fully plugged in.
- If you want to use the additional mounting bracket for the TTL digital I/Os choose two slots side by side for installation. Remove (if neccessary) an additional blind bracket for the slot.
- Screw all mounting brackets.
- Close the housing as described in the manual of your PC system

2.2 Software installation

2.2.1 Installation under Windows

The ALLDAQ driver system is installed with a comfortable installation routine (optionally as 32 bit or 64 bit package). Run the file *ALLDAQDriverSetup32.exe* for 32 bit systems resp. *ALLDAQDriverSetup64.exe* for 64 bit systems in the target directory of your download. Device drivers, programs, the Software Developer Kit (SDK), help files, manuals and if necessary, further software components will be installed. The "Advanced" option allows you to select individual installation components, such as Virtual Instruments (VIs) for your LabVIEW installation. You can install and uninstall individual components at any time via the Windows Control Panel.

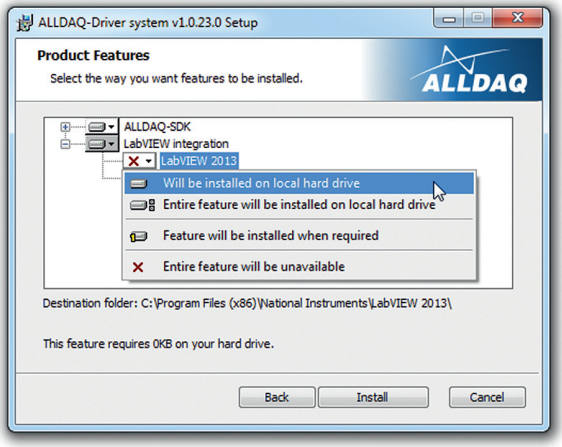


Figure 10: Installation program

After installation is complete, the ALLDAQ Launcher will start. The system tray icon - usually in the bottom right corner of the screen - allows you easy access to the ALLDAQ Manager, the Software Developer Kit (SDK), software tools, help files and manuals with the right mouse button. Alternatively, you can also access the ALLDAQ software from the Windows Start menu.

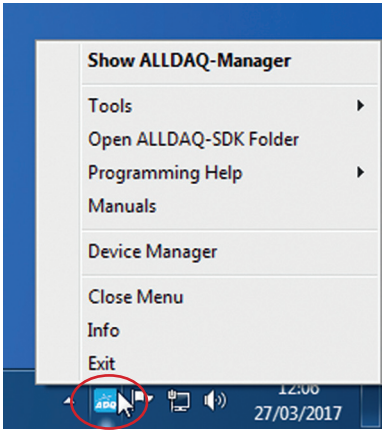


Figure 11: ALLDAQ-Launcher

2.3 Test programs

The ALLDAQ SDK contains simple command line and test programs with graphical user interface. For Visual C++, you will find the most extensive collection of sample programs with program code and the corresponding executables that you can use to test the board in the subdirectory "Applications".

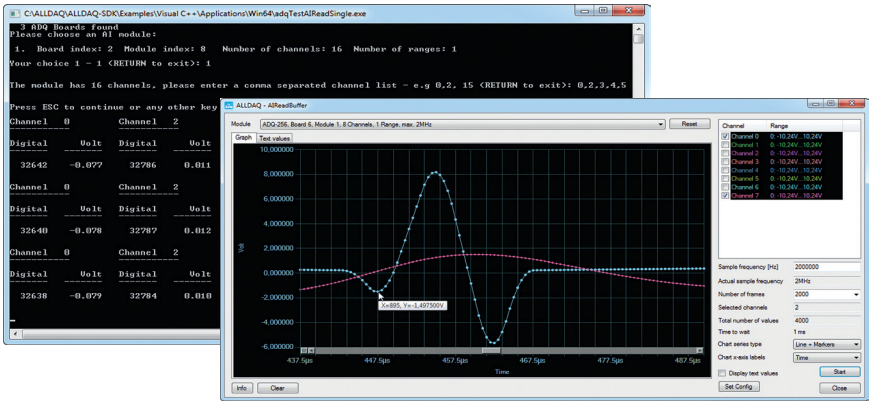


Figure 12: Command line program (left), test program with user interface (right)

2.4 Adjustment/calibration

Basically you can choose by the ALLDAQ Manager which adjustment data record (factory or user) should be activated on boot. You can change the setting anytime by the ALLDAQ Manager.

The setting can be found under "Tools - Adjustment AI" resp. "Adjustment AO". With "Adjustment on Boot" you can select the dataset to be loaded when booting the computer. Each analog channel can be individually adjusted.

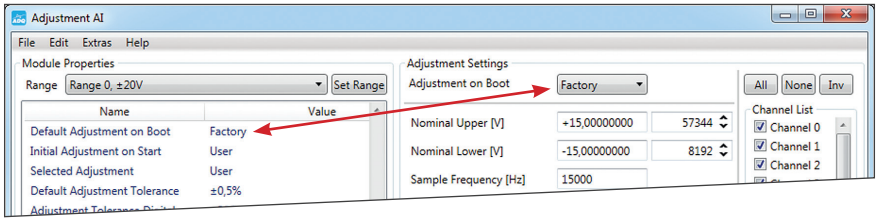


Figure 13: Adjustment settings

2.4.1 Factory adjustment

The boards of the ADQ-330/340 series will be adjusted before delivery. The adjustment data will be stored on the hardware. If a new factory adjustment should be neccessary please contact our service department. For contact details see chapter 4.4 on page 73.

2.4.2 User adjustment

To compensate for potential voltage drops caused by the field wiring, you as the user can carry out an adjustment of the analog inputs and outputs yourself. The generated correction data is stored on the hardware in addition to the factory adjustment data.

In the chapter "Adjustment Procedure" of the ALLDAQ Manager help file, a step-by-step guide describes the exact procedure for analog input and output channels.

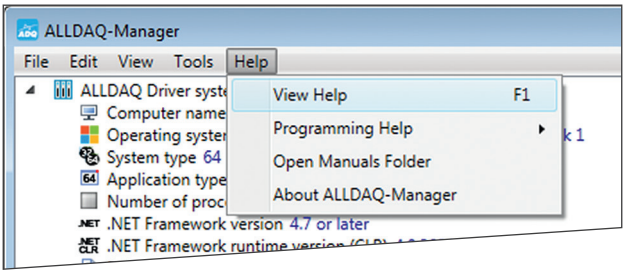


Figure 14: Adjustment procedure

2.4.2.1 Analog inputs

For a detailed description of the procedure, refer to the chapter "Adjustment AI" in the ALLDAQ Manager's help file (see Figure 14). Basically applies:

1. Power-on the system with the ADQ-330/340 series.
2. Connect the part of the field wiring you want to include into the adjustment.
3. Apply a constant voltage to one channel after the other and monitor the voltage by a high-precision voltmeter (e. g. multimeter). Make sure, that the voltmeter has a higher accuracy than the accuracy of your board. See also Figure 16.
4. Run the adjustment procedure for analog inputs in the ALLDAQ-Manager under "Tools - Adjustment AI" and follow the instructions in the help file.

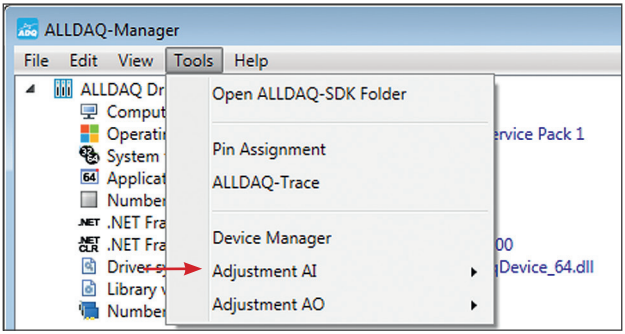


Figure 15: Adjustment analog inputs

TIP: To achieve the best accuracy, we recommend to set that sample rate which one you want to use in your measurement later.

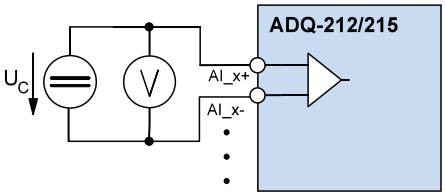


Figure 16: Adjustment wiring for analog inputs

2.4.2.2 Analog outputs

For a detailed description of the procedure, refer to the chapter "Adjustment AO" in the ALLDAQ Manager's help file (see fFigure 14). Basically applies:

1. Power-on the system with the ADQ-330/340 series.
2. Connect the part of the field wiring you want to include into the adjustment.
3. Run the adjustment procedure for analog outputs in the ALLDAQ-Manager under "Tools - Adjustment AO" and follow the instructions in the help file.

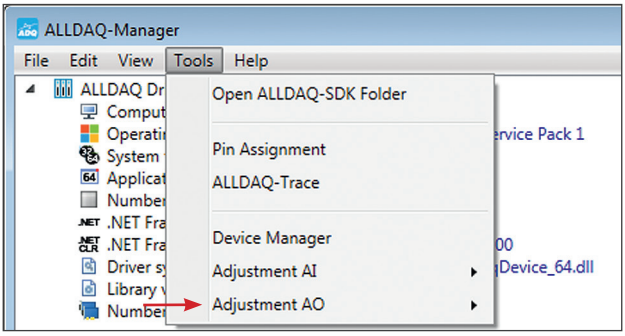


Figure 17: Adjustment analog outputs

4. The adjustment procedure outputs a constant voltage at the respective output AO_y, which you have to measure with a high-precision voltmeter (e. g. multimeter). Note that the voltmeter must always have a better accuracy than the board to be adjusted.
5. Now enter the measured value in the corresponding field of the adjustment procedure. Details are described in the help file.

Note: Repeat the adjustment for each channel separately.

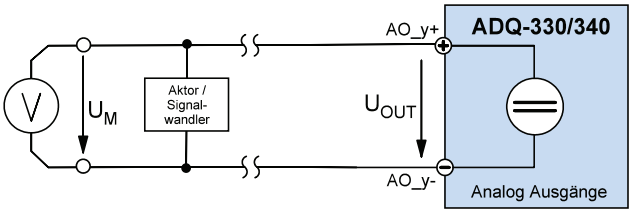


Figure 18: Adjustment wiring for analog outputs

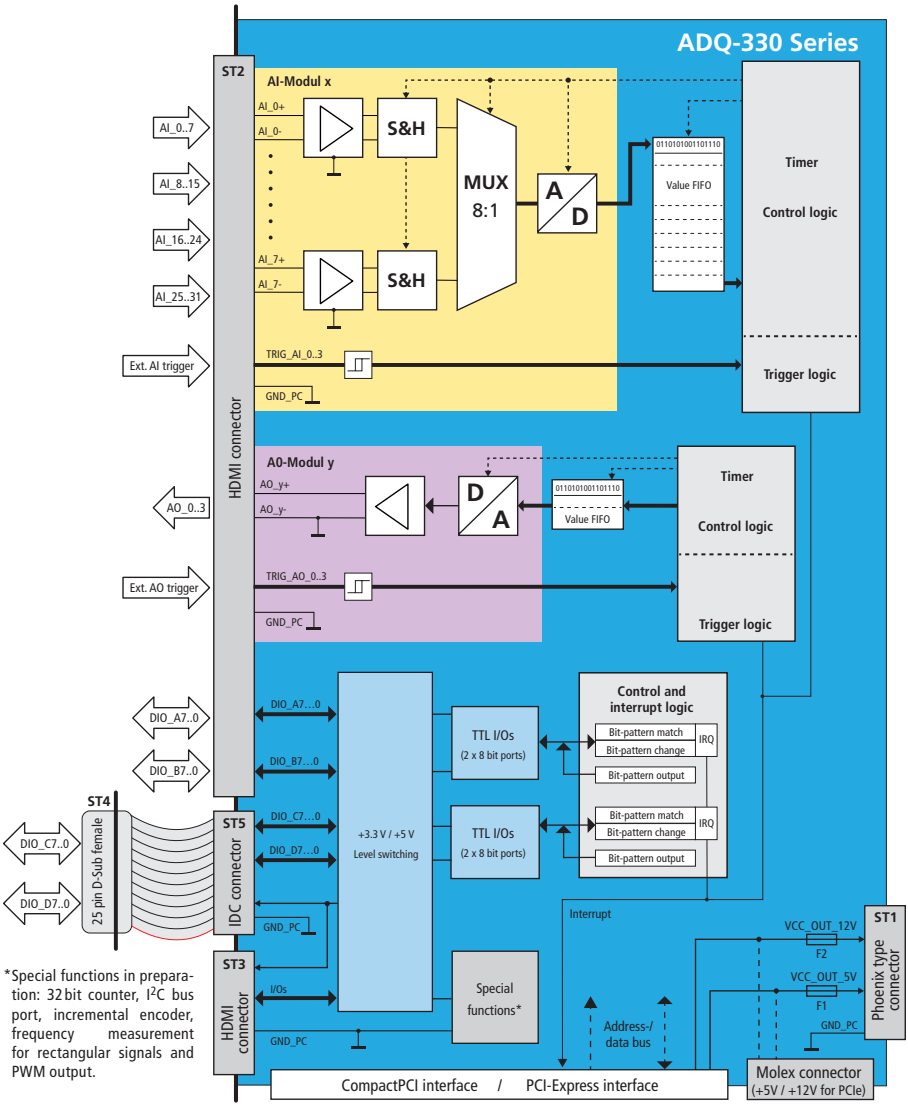
2.4.3 DAkkS calibration

For issuing calibration certificates we cooperate with independent test laboratories accredited by the Deutsche Akkreditierungsstelle GmbH (DAkkS). On demand please contact our service department. For contact details see chapter 4.4 on page 73

3. Functional groups

3.1 Block diagrams

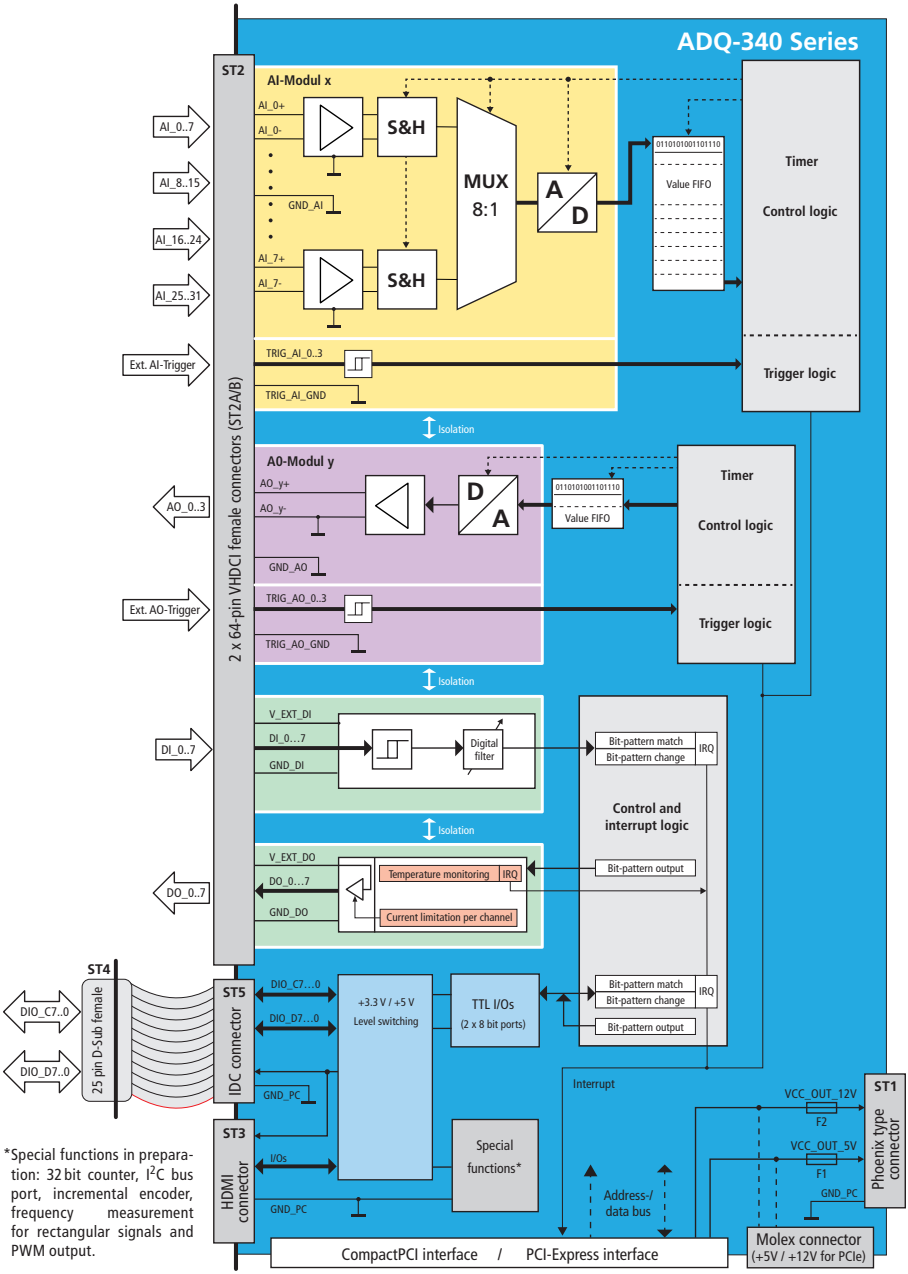
3.1.1 Block diagram ADQ-330 series



*Special functions in preparation: 32 bit counter, I²C bus port, incremental encoder, frequency measurement for rectangular signals and PWM output.

Figure 19: Block diagram ADQ-330 series

3.1.2 Block diagram ADQ-340 series



*Special functions in preparation: 32 bit counter, I²C bus port, incremental encoder, frequency measurement for rectangular signals and PWM output.

Figure 20: Block diagram ADQ-340 series

3.2 Analog acquisition

Analog inputs of the e Eingänge der ADQ-330/34ADQ-330/340 series in overview:

	ADQ-331/341	ADQ-332/342	ADQ-334/344
Channels	2 x 8 pseudo-differential	2 x 8 pseudo-differential	4 x 8 pseudo-differential
Resolution	18 bit		
Bandwidth (-3 dB)	96 kHz		
Common mode rejection	128 dB between adjacent channels		
Sample rate	200 kS/s up to 800 kS/s synchronous (1 channel: 800 kS/s, 2 channels: 550 kS/s, 8 channels: 200 kS/s)*		
Input range	±10.24 V, ±5.12 V, 0..10.24 V, 0..5.12 V (0-20 mA on request)		
Input impedance	R_{IN} = 100 MΩ || C_{IN} = 680 pF		

Table 3: Analog inputs in overview

The models ADQ-331, ADQ-332, ADQ-341 and ADQ-342 provide 16 pseudo-differential input channels, the ADQ-334 and ADQ-344 provide 32 pseudo-differential input channels. In the case of pseudo-differential transmission, the positive and negative signal lines are routed separately in our case, but connected to ground of the board via 100 MΩ each. In the case of non-isolated models, this is the PC ground, in the case of isolated models, the separate ground of the analog input section (GND_AI) serves as common reference potential for the analog inputs.

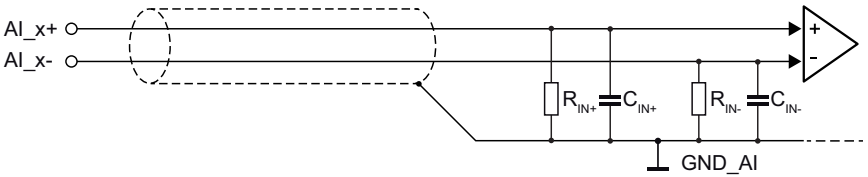


Figure 21: Pseudo-differential wiring Pseudo-differential wiring

The analog inputs are organized in channel groups of 8 channels each. In the software, a channel group is also referred to as a port with 8 channels each. Depending on the model a board has 2 or 4 channel groups resp. AI ports.

	ADQ-331/341	ADQ-332/342	ADQ-334/344
	AI channel number (pin naming)		
Port AI0	AI_0(±)…AI_7(±)	AI_0(±)…AI_7(±)	AI_0(±)…AI_7(±)
Port AI1	AI_8(±)…AI_15(±)	AI_8(±)…AI_15(±)	AI_8(±)…AI_15(±)
Port AI2	–	–	AI_16(±)…AI_23(±)
Port AI3	–	–	AI_24(±)…AI_31(±)

Table 4: Channel groups (AI ports)

The sampling rate can be set separately for each channel group (AI port). All channels are recorded synchronously, "frozen" in a sample-and-hold unit and "picked up" with an 8:1 multiplexer. Depending on the number of active channels used per port, the sampling rate per channel applies:

Number of channels	1	2	3	4	5	6	7	8
Sample rate	800 kS/s	550 kS/s	425 kS/s	350 kS/s	300 kS/s	250 kS/s	225 kS/s	200 kS/s

Table 5: Dependency of the sample rate from number of channels

Synchronization of several AI ports is possible via software or external trigger.

The input voltage range is programmed per channel by software.

Nyquist-Shannon sampling theorem (Oversampling)

The Nyquist-Shannon sampling theorem tells us, that the sample rate for a periodic signal, whose maximum frequency component should be f_{Pmax}, must be at least twice as high, i. e. $2 \bullet f_{Pmax}$ or higher. In practice we recommend to choose a sampling rate by the factor 5 or 10 higher than f_{Pmax} to replicate the signal form truely. This issue is also called "oversampling".

Example:

The max. frequency component $f_{Pmax.}$ ($1/t_P$) of the signal frequency should be 25 kHz. The sample rate f_S ($1/t_S$) should be at least 5 x 25 kHz = 100 kHz.

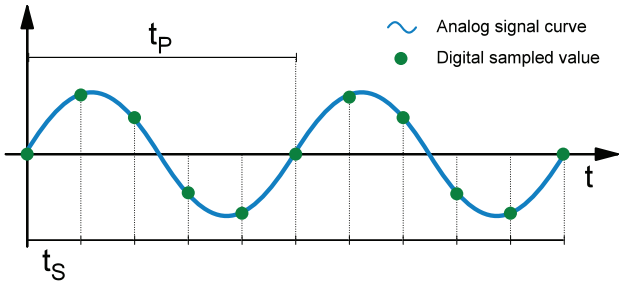


Figure 22: Nyquist-Shannon sampling theorem

3.2.1 Wiring

We recommend the use of the VHDCI cable with matching connection block, see chapter 4.3 on page 72.

3.2.1.1 Differential voltage inputs

A differential input only measures the potential difference between positive and negative input. Common mode interference is thus effectively suppressed. In our case, the positive and negative signal lines are routed separately, but connected to ground on the board via 100 MΩ each. This circuitry is also called pseudo-differential, see fFigure 17 on page 24. In non-isolated models, the PC ground (GND_PC) is the common reference potential; in isolated models, the separate ground of the analog input section (GND_AI) serves as the reference potential.

For the differential voltage U_{AI_x} applies: $U_{AI\_x} = (U_{AI\_x}+) - (U_{AI\_x}-)$.

Please note that the max. voltage between the analog inputs AI_x+ and AI_x- must not exceed the absolute value of 19 V_{pp}. Otherwise, irreversible damage to the board may occur.

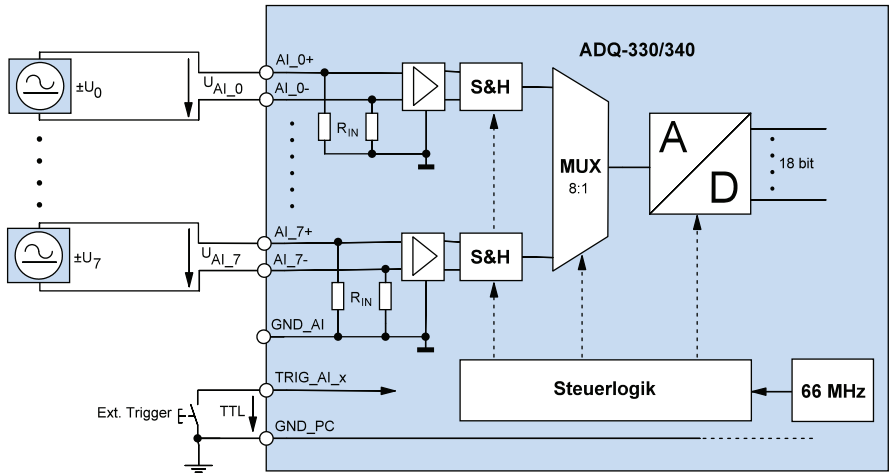


Figure 23: Differential voltage inputs

The input voltage ranges can be programmed for each channel. Depending on the application, select the smallest possible measuring range to benefit from the optimum resolution (sensitivity).

	Measuring range	Resolution (18 bit)	Accuracy
Range 0	-10,24 V..(+10,24 V-1 LSB)	1 LSB = 78,1 µV	±0,0146%
Range 1	0 V..(+10,24 V-1 LSB)	1 LSB = 39,0 µV	±0,0126%
Range 2	-5,12 V..(+5,12 V-1 LSB)	1 LSB = 39,0 µV	±0,018%
Range 3	0 V..(+5,12 V-1 LSB)	1 LSB = 19,5 µV	±0,017%

Table 6: Input ranges

3.2.1.2 External trigger AI section

All models of the ADQ-330/340 series provide a digital trigger input for each channel group (AI port). Depending on configuration the conversion can be started by a rising, a falling or any of both edges.

- Port AI0 (Inputs: AI_0..7): TRIG_AI_0 (Pin B50)
- Port AI1 (Inputs: AI_8..15): TRIG_AI_1 (Pin B16)
- Port AI2 (Inputs: AI_16..23): TRIG_AI_2 (Pin B48)
- Port AI3 (Inputs: AI_24..31): TRIG_AI_3 (Pin B14)

3.2.1.2.1 Non-isolated models

The digital trigger inputs are designed for a TTL high level of +5V. The trigger signals require a reference to PC ground (GND_PC).

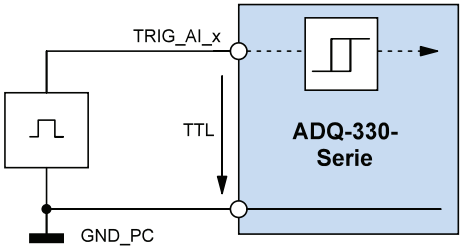


Abb. 24: Wiring of the not-isolated trigger inputs AI section

3.2.1.2.2 Isolated models

The digital trigger inputs are designed for a TTL high level of +5V. The trigger signals require a reference to TRIG_AI_GND as a common ground.

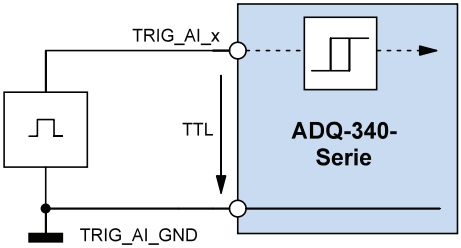


Abb. 25: Wiring of the isolated trigger inputs AI section

3.2.2 Programming

The analog inputs are combined into channel groups (AI ports) with eight channels each and are addressed in the software via a module index. Each model has either two or four AI ports.

When programming the analog acquisition, a differentiation is made between "single value acquisition" and "timer-controlled acquisition", depending on the application.

Refer to the procedure described in the online help.

3.2.2.1 Single value acquisition

This operation mode is for acquiring single values from one channel without fixed time reference.

Depending on configuration the conversion can be started by software or by a rising, falling or any edge at the external trigger input of the appropriate AI port (TRIG_AI_*x*).

3.2.2.2 Timer-controlled acquisition

With the timer-controlled acquisition you can sample signals in defined time intervals. You can acquire a pre-defined number of frames or continuously. The so-called value FIFO serves as a fast buffer memory to enable a continuous data transfer to the PC. The channel multiplexer is controlled by a channel-list, which can include 32 entries maximum.

Depending on configuration the conversion can be started either by software or by a rising, falling or any edge at the external trigger input of the appropriate AI port (TRIG_AI_*x*).

The following figure shows eight channels of an AI port, which are always scanned synchronously. Synchronization of the acquisition across multiple ports is possible by appropriate programming.

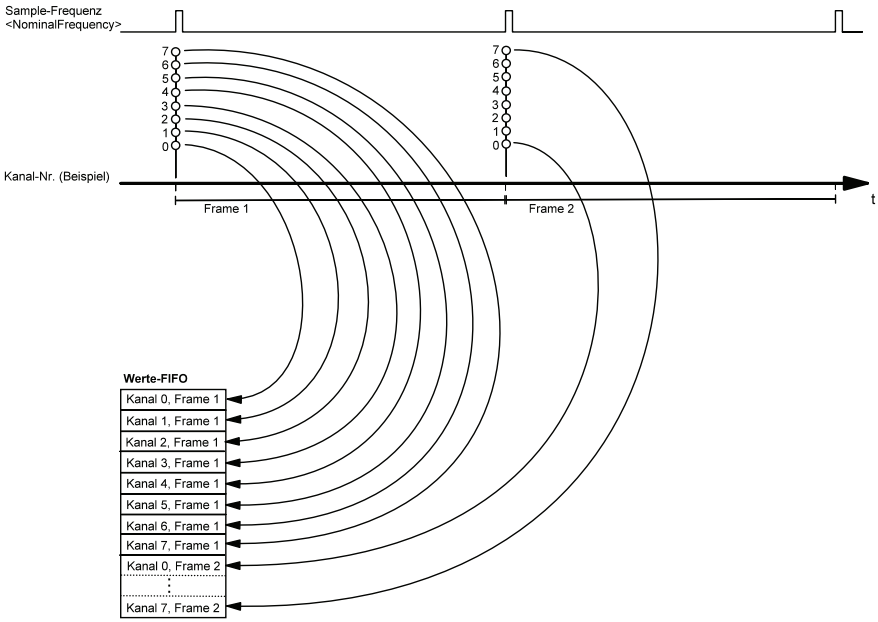


Figure 26: Timer-controlled acquisition

The dependency of the max. sample rate from the number of channels used per AI port you can find on page 28.

3.3 Analog output

3.3.1 Voltage outputs

Depending on the version, the ADQ-330/340 series multi I/O boards are equipped without, with 2 or 4 analog outputs, which are galvanically isolated from PC ground and the other function groups up to 1500 VDC (60 s). Each channel is equipped with a 500 kHz D/A converter with 16 bit resolution. The output voltage range exceeds ±10.24 V and automatically outputs a 0 V level after power-up.

The values can be output individually or timer-controlled. The output can be started by software or an external trigger signal either independently per channel or several channels synchronously. Each analog channel has its corresponding external digital trigger input (TRIG_AO_*y*), which is isolated towards PC ground and the other function groups.

Analog outputs of ADQ-330/340 series in overview:

	ADQ-331/341	ADQ-332/342	ADQ-334/344
Channels	--	2 voltage outputs	4 voltage outputs
Resolution	16 bit		
Output voltage range	±10.24 V		
Output rate	500 kS/s synchronous		
Output current	±15 mA per output		
Total accuracy	±2 LSB (±0.6 mV) ???		

Table 7: Overview analog outputs

Tip: With the utility program "WriteBufferAO" you can easily output the following pre-defined waveforms:

- Rectangular
- Sine
- Triangular
- Saw tooth rising/falling
- Sinc function
- Sine with phase control
- Sinusoid modulated rectangular
- Sweep signal
- NRZ-coded signal

If necessary, the fundamental oscillation can be superimposed with either Gaussian noise or white noise. In addition, a user-definable arbitrary signal can be generated via CSV file.

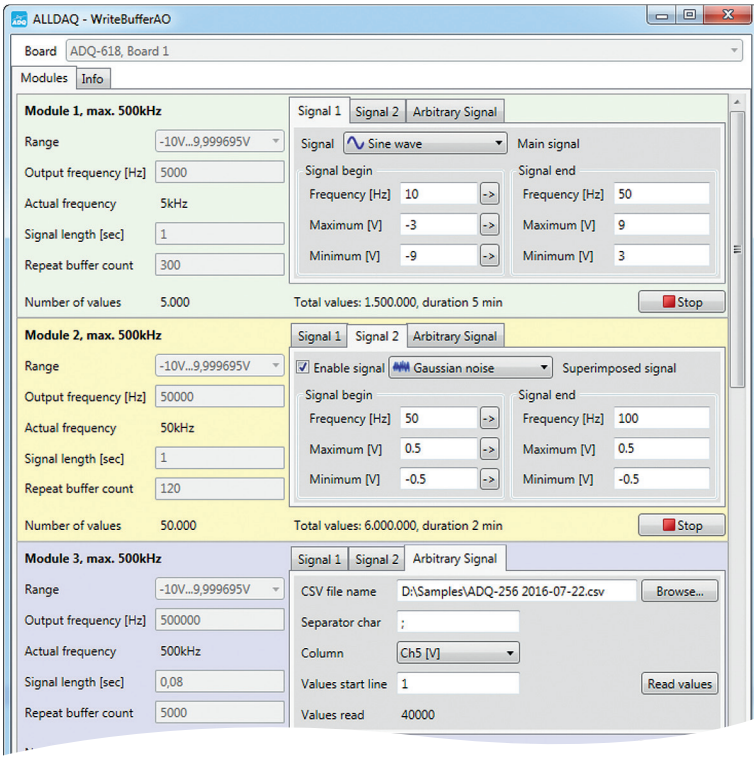


Figure 27: Utility program "WriteBufferAO"

3.3.2 Wiring

We recommend the use of the VHDCI cable with matching connection block, see chapter 4.3 on page 72.

3.3.2.1 Output voltage range

The output voltage range is ±10.24 V. The load for each channel is 15 mA max. The capacitive load at the output should not exceed 1 nF to ensure a stable signal. Individual modifications of the output stage on request.

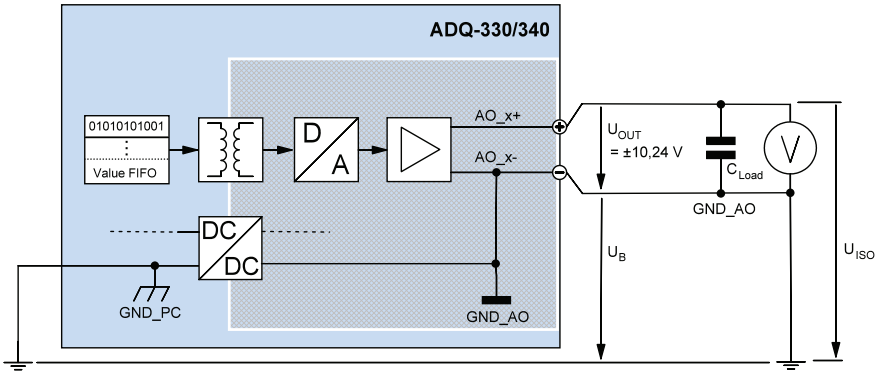


Figure 28: Output stage

The Total Harmonic Distortion (THD) defines the ratio between the accumulated harmonics power P_H to the power of the basic oscillation P_1. The THD of the ADQ-330/340 series output stage is specified with -96 dB and refers to a sine oscillation of 100 kHz with an amplitude of 10 V_{PP}.

3.3.2.2 External trigger AO section

The ADQ-332 and ADQ-342 provide two digital trigger inputs and the ADQ-334 and ADQ-344 provide four digital trigger inputs. This means that one digital trigger input is available for each analog output (AO port). Depending on configuration the output operation can be started or stopped by a rising, falling or any edge.

- Port AO0 (Output: AO_0): TRIG_AO_0 (Pin B40)
- Port AO1 (Output: AO_1): TRIG_AO_1 (Pin B6)
- Port AO2 (Output: AO_2): TRIG_AO_2 (Pin B42)
- Port AO3 (Output: AO_3): TRIG_AO_3 (Pin B8)

3.3.2.2.1 Not-isolated models

The digital trigger inputs are designed for a TTL high level of +5 V. The trigger signals require a reference to the PC ground (GND_PC).

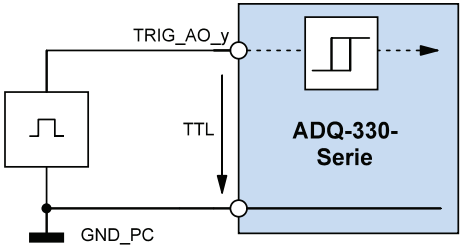


Figure 29: Wiring of the not-isolated trigger inputs AO section

3.3.2.2.2 Isolated models

The digital trigger inputs are designed for a TTL high level of +5 V. The trigger signals require a reference to TRIG_AO_GND as a common ground.

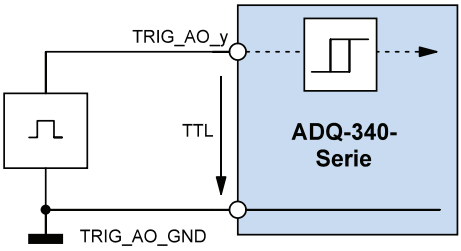


Figure 30: Wiring of the not-isolated trigger inputs AO section

3.3.3 Programming

The analog outputs are considered in the software as AO ports with one channel each and are addressed via a module index. This means that the models ADQ-332 and ADQ-342 have two AO ports and the models ADQ-334 and ADQ-344 have four AO ports.

For programming the analog outputs, you can choose between "Single value output" and "Timer controlled output", depending on the application. All channels can be started independently or synchronously via software or external trigger signal.

Please note the order of operation as described in the online help.

3.3.3.1 Single value output

This operation mode is for output of single values without fixed time reference.

Depending on the configuration the output can be started either by software or by a rising and/ or falling edge at the corresponding external trigger input (TRIG_AO_y).

3.3.3.2 Timer-controlled output

With the timer-controlled output you can output signal curves continuously. The so-called value FIFO serves as a fast buffer memory per channel which enables a continuous operation of all channels at maximum output rate.

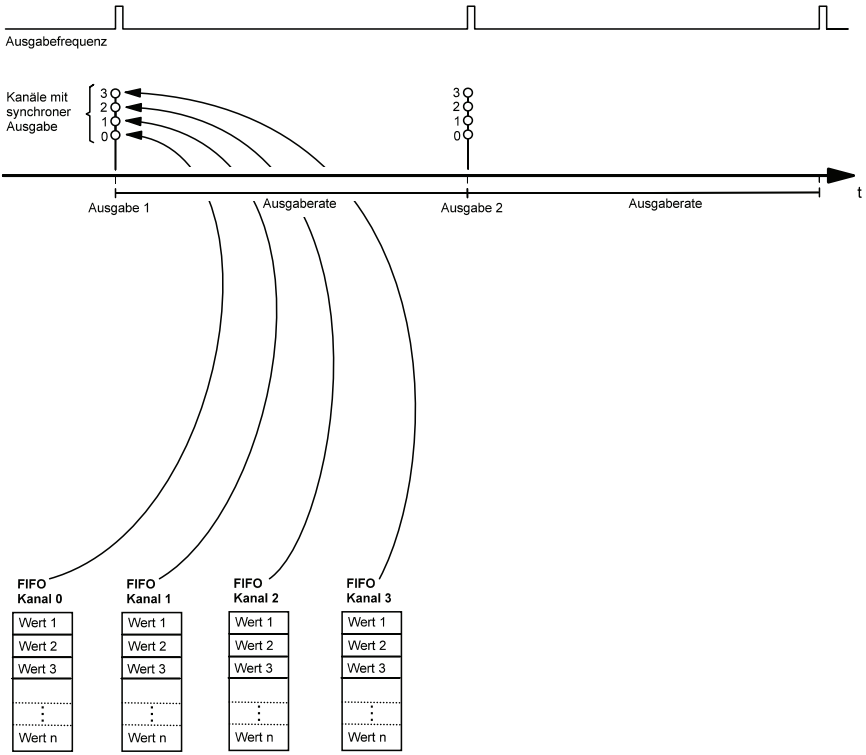


Figure 31: Timer-controlled output

3.4 Isolated digital inputs

The **ADQ-340 series** provides an isolated digital input port with 8 bits. The isolated inputs have a Schmitt trigger characteristic according to IEC 61131-2 (type 1) and are designed for a maximum input voltage of 35 V. The isolation voltage against PC ground is 500 VAC_{RMS} according to EN60664-1 resp. UL1577.

On demand all inputs can be monitored on bit-pattern change or bit-pattern match and can be evaluated as interrupt event. Additionally an interrupt can be generated if the voltage of the external supply is too low (V_EXT_DI < 8 VDC) or missing (V_EXT_DI < 12,1 VDC).

3.4.1 Digital input filter

To prevent undesirable effects like bouncing you can program a digital filter for the input port. Choose between the following values:

10 ms (N = 1248) / 3.2 ms (N = 400) / 1.0 ms (N = 125) / 10 µs (bypass). The scan frequency is 100 kHz (typ.).

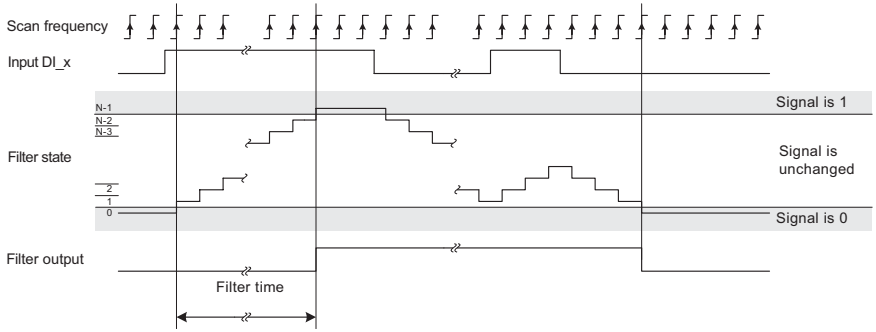


Figure 32: Digital input filter

3.4.2 Wiring

The isolated inputs have a Schmitt trigger characteristic according to IEC 61131-2 (type 1) and are dimensioned for a high-level U_{IH} of typ. 24 VDC as used in industrial control engineering. Please note the following conditions:

- Threshold voltage L → H: > 15 VDC @ V_EXT_DI = 24 VDC
- Threshold voltage H → L: < 11 VDC @ V_EXT_DI = 24 VDC
- Hysteresis: typ. 1 VDC

The external power supply V_EXT_DI can be in the range of 9.6..35 VDC, we recommend 24 VDC. Please note that always a ground connection of the external wiring to the reference ground of the isolated digital inputs (GND_DI) must be done.

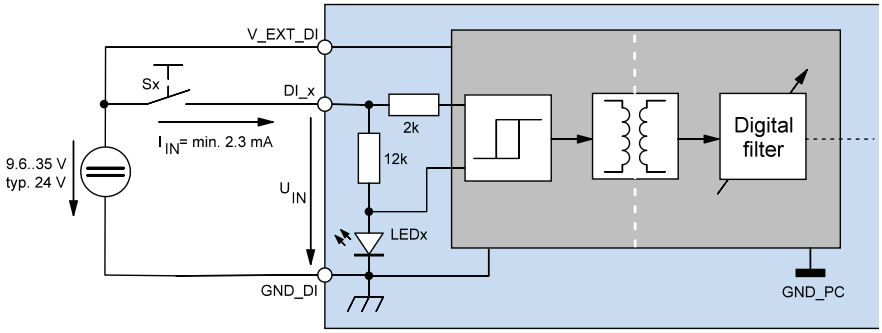


Figure 33: Wiring of the isolated digital inputs

3.4.3 Status LEDs

The isolated digital input port DI_x is equipped with 8 blue status LEDs. The assignment of the individual bits is shown in the following figure.

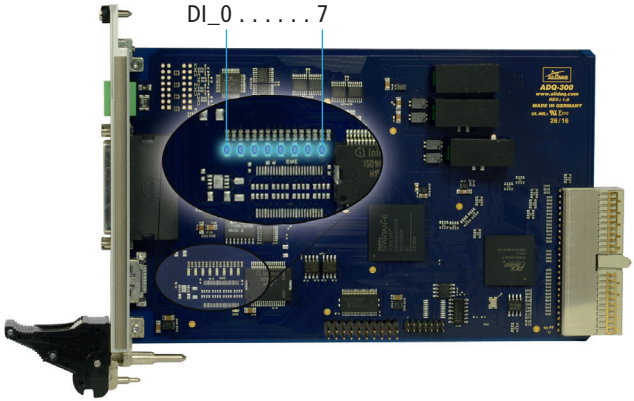


Figure 34: Status LEDs of the isolated digital inputs

3.4.4 Programming

The input port DI_x is 8 bit wide. It is addressed in the software via a module index. The port direction is fixed by the hardware. For the port a digital filter can be programmed: 10 ms / 3.2 ms / 1 ms / 10 µs (bypass) see chapter 3.4.1.

Please note the order of operation as described in the online help.

3.4.4.1 Simple reading

In this operation mode one digital value can be read with the appropriate port width.

3.4.4.2 Streaming operation

The software-controlled streaming operation enables a continuous reading of digital input ports with up to 10 kHz (depending on operation system and PC configuration).

3.4.4.3 Interrupt modes

On demand the isolated input port can be monitored on bit change or bit-pattern match and can be evaluated as an interrupt event. Additionally an interrupt can be generated on missing or too low external power supply. Programming is done in the operation mode „interrupt".

3.4.4.3.1 Bit change

In the operation mode „bit change" one or more input bits which should be monitored for toggling can be masked. For each rising and falling edge, a bit mask defines which bit and which edge should generate an interrupt. As soon as an appropriate edge at minimum one bit masked with „1" occurs, an interrupt is triggerd (see Figure 35).

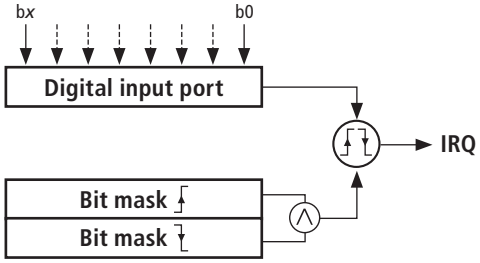


Figure 35: Bit change

Example for bit change:

The names mentioned for variables, structures and functions apply to C++ and may vary slightly depending on the programming language.

- When passing the value FFHex in the member variable `uiPortBitChangeRisingEdge` of the structure `SADQIRQEnable` in function `adqEnableIRQ()` all bits of a port are monitored on a rising edge for example. If only single bits should be monitored (e. g. monitoring of bit b2 on rising edge), the corresponding bit of the bit mask must be set to „1" (e. g. `uiPortBitChangeRisingEdge = 0x4`).
- An interrupt is triggered as soon as a rising edge at bit b2 is detected.
- For evaluation of the interrupt event use the member variables `uiPortBitChangeRisingEdge` resp. `uiPortBitChangeFallingEdge` of the structure `SADQIRQStatus` in the function `adqWaitIRQ()`. You get the information which bit with which edge (rising/falling) triggered the interrupt.

3.4.4.3.2 Bit-pattern compare

In the operation mode „bit-pattern compare" a pre-defined reference bit-pattern is compared with the bit-pattern attached to the corresponding input port. On bit-pattern match an interrupt is triggered (see Figure 36).

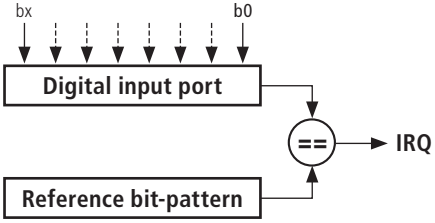


Figure 36: Bit-pattern compare

Example for bit-pattern compare:

The names mentioned for variables, structures and functions apply to C++ and may vary slightly depending on the programming language.

- With the member variable `uiPortBitPatternValue` of the structure `SADQIRQEnable` the reference bit-pattern is defined. Next the structure will be passed to the function `adqEnableIRQ()`.
- Enable the interrupt passing the boolean value TRUE in member variable `bPortBitPatternCompare` of the structure `SADQIRQEnable` in function `adqEnableIRQ()`.
- As soon as all bits at the input port match the reference bit-pattern an interrupt is triggered.
- For evaluation of the interrupt event use the member variable `bPortBitPatternCompare` of the structure `SADQIRQStatus` in the function `adqWaitIRQ()`. TRUE indicates that bit-pattern match occured.

3.4.4.3.3 Power supply missing

On demand an interrupt can be generated if the external power supply (V_EXT_DI < 12,1 V) is missing.

3.4.4.3.4 Power supply too low

On demand an interrupt can be generated if the external power supply (V_EXT_DI < 8 V) is too low.

3.5 Isolated digital outputs

The **ADQ-340 series** provides an isolated digital output port with 8 bits. The outputs are assembled with a power FET which can drive up to 0.6 A per channel. The isolation voltage against PC ground is 500 VAC_{RMS}.

3.5.1 Wiring

The outputs are dimensioned for a high level of 24 VDC (U_{OH} = 11..35 VDC) as used in industrial control engineering. The max. output current is I_O = 0.6 A per channel. To increase the output current connecting the outputs in parallel is possible. A ground reference to the external output wiring must be done by GND_DO.

The output stage offers an extensive overload protection:

- Short-circuit-proof outputs (current limitation per channel)
- Shutdown on current peaks of typ. 1.4 A, e. g. with inductive loads
- Over-voltage protection for V_EXT_DO > 47 VDC
- Under-voltage shutdown: V_EXT_DO = min. 7 VDC / max. 10.5 VDC, restart at max. 11 VDC, hysteresis: typ. 0.5 VDC
- Thermal shutdown with automatic restart. In overload condition (T_{TSD} = typ. 135°C) channel turns OFF and back ON automatically as soon as the junction temperature decreased by 10 °K. In overload state the output driver can send an interrupt to the PC (per port).

For supply of the output drivers an external power supply must be connected to the V_EXT_DO pins sourcing sufficient power. In case of full load it is max. 9.6 A for the ADQ-340 series.

Attention: the 68-pin VHDCI connector (ST2A/B) can grow warm!

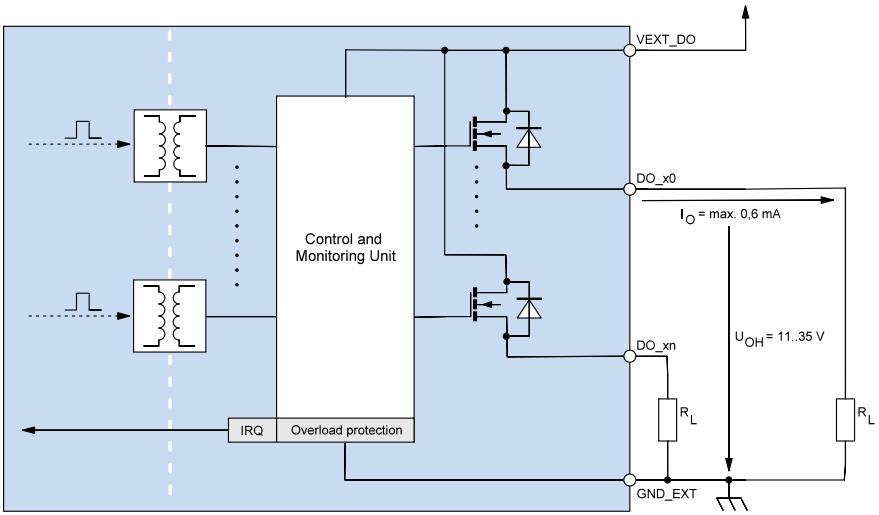


Figure 37: Wiring of the isolated digital outputs

3.5.2 Programming

The output port DO_x is 8 bit wide. It is addressed in the software via a module index. The port direction is fixed by the hardware.

Please note the order of operation as described in the online help.

3.5.2.1 Simple output

In this operation mode one digital value can be output in the given port width.

Note: An output port can be read back also!

3.5.2.2 Streaming operation

The software-controlled streaming operation enables the output of a bit pattern stream by port with up to 10 kHz (depending on operation system and PC configuration).

3.5.2.3 Interrupt modes

On overload of the output driver the affected port will be shutdown automatically and an interrupt is triggered.

3.6 Bi-directional digital I/Os

Depending on the model, the ADQ-330/340 series has up to four bi-directional 8-bit wide digital I/O ports whose direction can be changed port by port via software. The voltage level of all TTL digital I/Os can be switched together between +3.3 V and +5 V via software and thus adapted to your application. Each output can drive up to 20 mA.

If a digital port is configured as input, the inputs can be monitored for bit change and generate an interrupt. Streaming mode enables continuous polling or outputting of a bit pattern stream on all DI, DO and DIO ports up to about 10 kHz (depending on operating system and computer configuration).

Note: After power-up all bi-directional ports are configured as input.

ADQ-330 series

The boards of the non-isolated ADQ-33x models are equipped with 32 TTL digital I/Os, of which the ports DIO_Ax and DIO_Bx are located on the two 68-pin VHDCI sockets ST2A/B. The ports DIO_Cx and DIO_Dx can be used via ST5 if required.

ADQ-340 series

The ADQ-34x models have two isolated ports routed to the two 68-pin VHDCI sockets ST2A/B. In this case, port DIO_Ax is the isolated digital input port (see chapter 3.4) and port DIO_Bx is the isolated digital output port (see chapter 3.5). The remaining 16 TTL digital I/Os, which are connected to ST5 as in the ADQ-330 series, are addressed as port DIO_Cx and DIO_Dx.

For access to port DIO_Cx and DIO_Dx there is an additional front panel for cPCI slots in the cPCI models and an additional mounting bracket for PCI-Express models (pin-out see page ??).

3.6.1 Wiring

When wiring the inputs and outputs take care that the TTL level is met (see specifications on page 62) and that a reference to PC ground (GND_PC) must be established. The max. output current is $I_O = I_{OL} = I_{OH} = 20\,mA$.

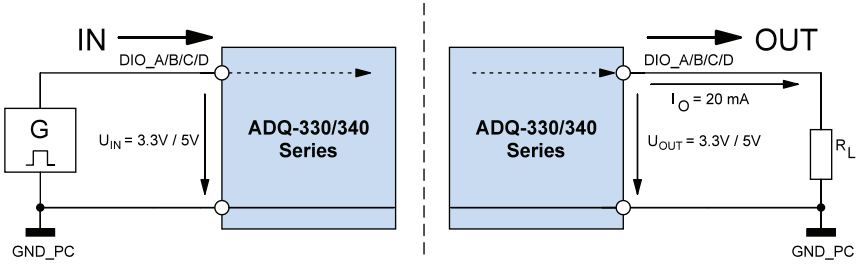


Figure 38: Wiring of the bi-directional digital I/Os

The ports DIO_A and DIO_B are not available on the isolated models (ADQ-34x).

3.6.2 Programming

The four digital I/O ports (DIO_Ax, DIO_Bx, DIO_Cx, DIO_Dx) can be programmed port by port (8 bit wide) as input or output. They are addressed in the software via a module index. After power-up all bi-directional ports are configured as input.

Follow the order of operation as described in the online help.

3.6.2.1 Simple input/output

In this operation mode one digital value of the appropriate port can be read resp. output. The port direction is defined by software.

Note: A port configured as output can be read back also!

3.6.2.2 Streaming operation

Depending on the port direction the software-controlled streaming operation enables a continuous reading of digital inputs resp. the output of a bit pattern stream with up to 10 kHz (depending on operation system and PC configuration).

3.6.2.3 Interrupt modes

On demand a digital I/O port configured as input can be monitored on bit change or bit-pattern match and can be evaluated as an interrupt event. Programming is done in the operation mode „interrupt".

3.6.2.3.1 Bit change

In the operation mode „bit change" one or more input bits which should be monitored for toggling can be masked. For each rising and falling edge, a bit mask defines which bit and which edge should generate an interrupt. As soon as an appropriate edge at minimum one bit masked with „1" occurs, an interrupt is triggerd (see Figure 39).

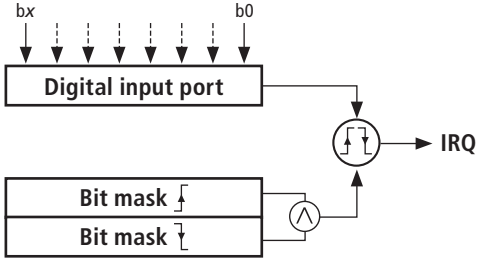


Figure 39: Bit change

Example for bit change:

The names mentioned for variables, structures and functions apply to C++ and may vary slightly depending on the programming language.

- When passing the value FFHex in the member variable `uiPortBitChangeRising-Edge` of the structure `SADQIRQEnable` in function `adqEnableIRQ()` all bits of a port are monitored on a rising edge for example. If only single bits should be monitored (e. g. monitoring of bit b2 on rising edge), the corresponding bit of the bit mask must be set to „1" (e. g. `uiPortBitChangeRisingEdge = 0x4`).
- An interrupt is triggered as soon as a rising edge at bit b2 is detected.
- For evaluation of the interrupt event use the member variables `uiPortBitChange-RisingEdge` resp. `uiPortBitChangeFallingEdge` of the structure `SADQIRQ-Status` in the function `adqWaitIRQ()`. You get the information which bit with which edge (rising/falling) triggered the interrupt.

3.6.2.3.2 Bit-pattern compare

Note: The operation mode bit-pattern compare is not available for ADQ-334 and ADQ-344.

In the operation mode „bit-pattern compare" a pre-defined reference bit-pattern is compared with the bit-pattern attached to the corresponding input port. On bit-pattern match an interrupt is triggered (see Figure 40).

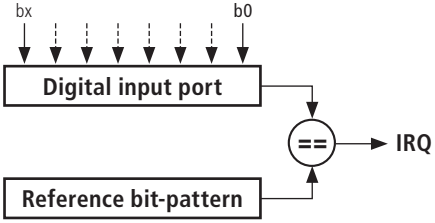


Figure 40: Bit-pattern compare

Example for bit-pattern compare:

The names mentioned for variables, structures and functions apply to C++ and may vary slightly depending on the programming language.

- With the member variable `uiPortBitPatternValue` of the structure `SADQIRQ-Enable` the reference bit-pattern is defined. Next the structure will be passed to the function `adqEnableIRQ()`.
- Enable the interrupt passing the boolean value TRUE in member variable `bPortBit-PatternCompare` of the structure `SADQIRQEnable` in function `adqEnable-IRQ()`.
- As soon as all bits at the input port match the reference bit-pattern an interrupt is triggered.
- For evaluation of the interrupt event use the member variable `bPortBitPattern-Compare` of the structure `SADQIRQStatus` in the function `adqWaitIRQ()`. TRUE indicates that bit-pattern match occured.

3.7 Special Functions

Special functions such as 32 bit counter, I^2C bus port, incremental encoder (in preparation), frequency meter for square wave signals and PWM output.

3.7.1 Wiring

The inputs and outputs of the special functions are routed to the HDMI connector ST3. For pin assignment see page <?>. The voltage level of all special I/Os can be switched together with the TTL digital I/Os between +3.3 V and +5 V by software.

When wiring the inputs and outputs take care that the TTL level is met (see specifications on page 62) and that a reference to PC ground (GND_PC) must be established. The max. output current is $I_O = I_{OL} = I_{OH} = 20\,mA$.

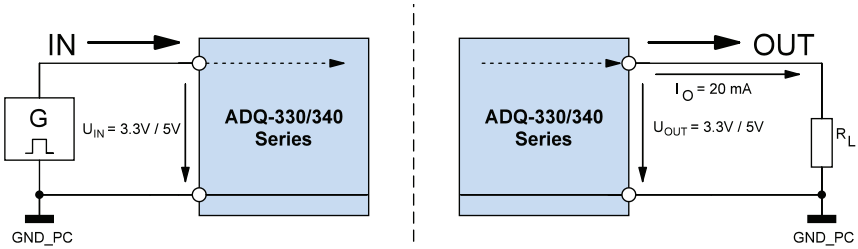


Figure 41: Wiring of the special I/Os

3.7.2 Description

3.7.2.1 Counter

The ADQ-330/340 series has a 32 bit down-counter with a wide range of settings. The counter always counts downwards with positive edge. The clocking is sourced either internally or externally with a square wave signal of up to 66 MHz. After switching on, the counter is set to zero. The Enable signal releases the counter and waits for the start signal. The counting process is triggered either by software start or by an external trigger signal, which must be present at least two clock periods. As soon as the zero crossing is reached, an interrupt is triggered and the strobe output goes to high for an adjustable duration (inverting is possible via software). After reaching zero, the counter starts counting down again in reload mode - if an individual start value has been passed, it is automatically reloaded. The counter can be reset at any time by software, the strobe output goes immediately to low level.

As a special feature, the counter offers the possibility to define a threshold value in the range between start value and zero. The threshold value is given as a multiple of the count rate and describes the distance from zero. As soon as the current count corresponds to the threshold value, an interrupt is triggered.

The following control signals and the counter output are available on the HDMI connector ST3:

- **Enable input** (CNT_EN, pin 14): Enabling the counter is always necessary. Either by this input or by software (then this input will be ignored).
  - Low level: Counter doesn´t start / stands still (level at the strobe output not affected).
  - High level: Counter starts / continuous counting.
- **External trigger input** (CNT_TRIG, pin 17): External trigger input for starting the counting process. If the counter has already elapsed, the start value is automatically reloaded and the counter is restarted.
  - Low level: The trigger pulse must be attached at least two clock periods. The counter starts synchronously with the next positive edge of the clock source.
  - High level: Counter is started by software.
- **External clock input** (CNT_EXT_CLK, pin 6): Switching between internal or external clock source via software.
  - Disabled: Clock source is the internal 66 MHz clock.
  - Enabled: The counter counts with the rising edge at this input.
- **Strobe output** (CNT_OUT, pin 4): Strobe pulse at zero crossing (invertible via software).

Features in overview:

- Start value (Preset) for 32 bit counter can be loaded.
- "Reload" mode for continuous counting. After zero crossing the start value is automatically reloaded. The counting continues without a break. If the mode is not activated, the counter stops at "zero".
- Interrupt on zero crossing.
- Interrupt on a programmable threshold. The Threshold must always be smaller than the start value and describes the distance from zero.
- Strobe outputs a pulse of variable length on zero crossing. The duration of the signal can be programmed as a multiple of the counter clock but must always be smaller than the start value. The output level is high active by default and can be inverted by software.
- Enabling the counter either by software or external enable input (CNT_EN).
- Start of the counter by software or external trigger pulse (CNT_TRIG). It must be attached a high level for at least two clock periods to reliably detect the trigger pulse. The counter starts synchronously with the next positive edge of the clock source.

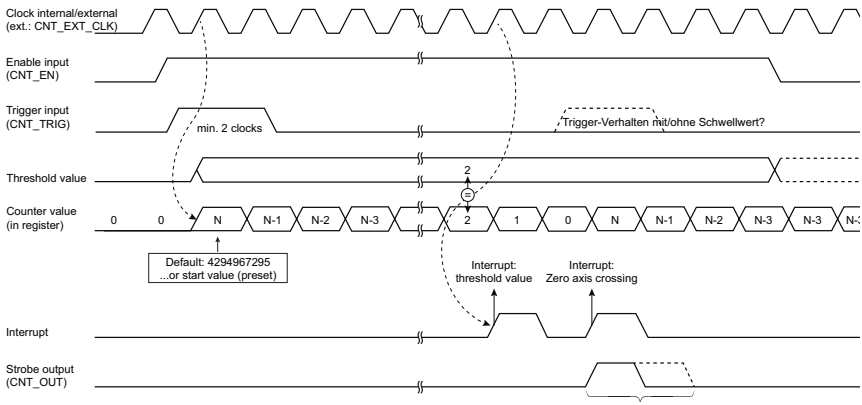


Figure 42: Timing 32 bit counter

3.7.2.2 I²C bus port

The ADQ-330/340 series has one I²C bus port, which is provided via the HDMI connector ST3. The I²C bus (Inter Integrated Circuits Bus) is a serial interface that requires only two lines. The clock line "Serial Clock" (I2C_SCL, pin 15) and the data line "Serial Data" (I2C_SDA, pin 16). The lines work bidirectionally. A distinction is made between master and slave for bus devices. The bus subscribers are addressed via I²C addresses, 128 subscribers per bus are possible. Individual bus subscribers can also assign several addresses. Please observe the procedure for setting the address ranges (e. g. with DIP switches) in the manual of the respective device.

Basically the I²C bus can be operated with different speeds:

Mode	Speed
Standard Mode (Sm)	0.1 Mbit/s (currently not supported)
Fast Mode (Fm)	0.4 Mbit/s
High Speed Mode (HS-Mode)	1.0 Mbit/s (currently not supported)
Ultra Fast Mode (UFm)	5.0 Mbit/s (currently not supported)

Table 8: I²C velocities

The I²C port of the ADQ-330/340 series is clocked at 400 kHz, i. e. the bus operates in fast mode. The modes of all bus devices must be identical. The master, i. e. the ADQ-330/340, determines the clock rate on the SCL line. The effective data are transmitted via the SDA line.

Note: The boards of the ADQ-330/340 series always operate as master. No further masters are allowed on the I²C bus.

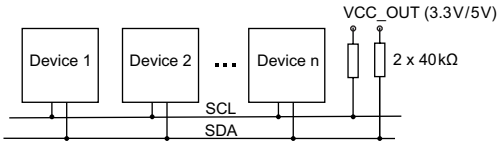


Figure 43: I²C bus structure

A maximum of 128 devices can be connected to an I²C bus, if each of the devices occupies only one address, otherwise correspondingly less. The devices are connected to each other via two bi-directional bus lines. The two pullup resistors with reference to VCC_OUT (3.3 V / 5 V) are already assembled on the ADQ-330/340 series.

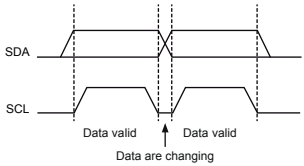


Figure 44: Valid data at the I²C bus

The clock indicates when valid data are present. You can see in Figure 44 that this is always the case with the high level of the SCL line. The receiver can now read and evaluate the data. The master specifies the clock rate, it then either creates its own data or expects it from the corresponding device.

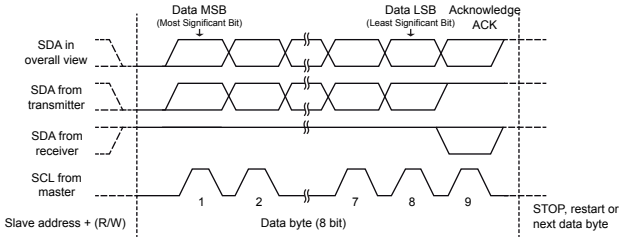


Figure 45: Data transfer at the I²C bus

In Figure 45 you can see the timing diagram of a data transfer with the following signals (from bottom up):

- The clock signal SCL (from master, here given from ADQ-330/340 series)
- The data line SDA in view of the receiver, not actively driven
- The data bits as sent out from the transmitter (low active)
- The SDA signal in an overall view (at the top)

Synchronization is important. A receiver (regardless of whether master or slave) sends an acknowledge signal (ACK = acknowledge) at the end of each data packet by pulling the SDA line

to low level. Since this corresponds to a low-active wired-OR, it is sufficient, if one slave sends the ACK signal.

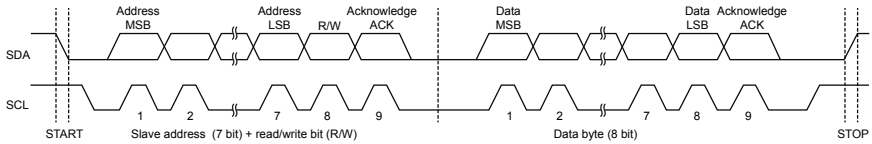


Figure 46: Complete transfer cycle at the I^2C bus

In Figure 46 you can see the whole transmission cycle. First, the master sends a packet with the receiver's address. The address consists of 7 bits, supplemented by another bit called R/W (Read/Write) bit as LSB. All bus subscribers compare the transmitted address with their own. If it matches, the appropriate slave acknowledges receipt with an ACK signal by briefly setting the SDA line to low. Depending on the R/W bit, the addressed slave knows whether it is to start a transmit or receive cycle. The effective data transfer can then begin. As a conclusion, a stop cycle is initiated. To do this, the clock is set to high and then the SDA line is enabled. The lines SDA and SCL are now both at high level so that a new cycle can be started. Up to 4 data bytes can be transferred per write or read cycle.

3.7.2.3 Incremental encoder port (in preparation, all details without guarantee)

The ADQ-330/340 series provides a quadrature encoder with a signed 16 resp. 17 bit up/down counter. Sensors that provide a digital, electrically bounce-free signal can be connected directly to the incremental encoder port. The signal level must be according to the TTL specification, see page Seite 62.

The following inputs are available on the HDMI connector ST3:

- **A-input** (INC_A, pin 10): Sensor input channel A
- **B-input** (INC_B, pin 12): Sensor input channel B
- **External reset input** (INC_EXT_RST, pin 19): Asynchronous reset immediately sets the counter to zero.

Functional principle

Incremental encoders are sensors for capturing changes in position (linear) or angle (rotary) that can detect distance and direction resp. angle variation and direction of rotation. The term incremental encoder is used here as a substitute for rotary sensors, quadrature encoders, rotary encoders or rotary pulse encoders. In automation technology, sensors are commonly used which output a digital signal in the Gray code.

The sensor must supply two 90° phase shifted square-wave signals according to Gray code at the output. A special counter implemented in the board's hardware detects the direction of movement by means of the phase shift of the two channels A and B (also called track A/B or quadrature signal) and counts the pulses for position determination.

The Gray code offers the advantage that only one bit changes between adjacent codes. The counting direction results from the sequence of the states of the 2-bit Gray code:

00 → 01 → 11 → 10

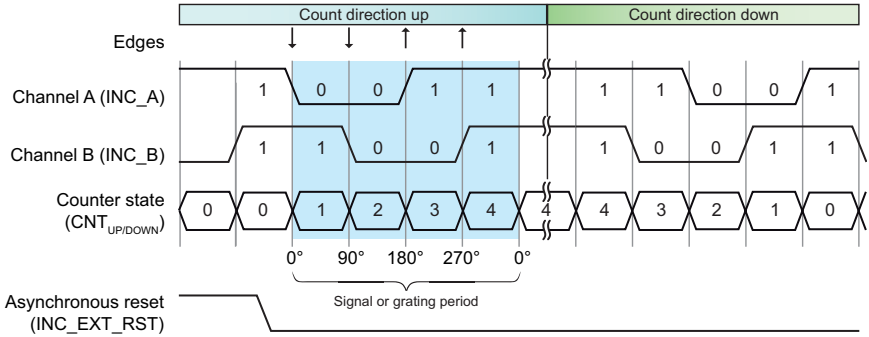


Figure 47: Functional principle of incremental encoder

Signal processing

When moving, the two channels A and B provide two signals that are 90° phase shifted. If the so-called measuring standard moves to the right, the signal from channel A is 90° ahead of that from channel B. In the other direction, the signal from channel A is 90° lagging behind that of channel B. The four gray-coded states of A and B are repeated with each signal period. Corresponding to the quadrants of a circular movement, the four steps are described with 0, 90, 180 and 270 degrees and are also summarized under the term grating period.

A special counter on the boards of the ADQ-330/340 series detects the direction and counts the pulses from these two signals. This allows you to directly deduce the distance respectively angle of the measuring standard. Speed and direction can be determined from the old (A_{OLD}/B_{OLD}) and the new state (A_{NEW}/B_{NEW}) and the time between the state changes of A and B. The implementation uses the so-called 4-fold resolution, which changes the counter at each edge (positive or negative) (see). However if you count only each signal period (4 steps) it is called a simple resolution.

If the incremental encoder is in the range of an edge, additional pulses can occur due to smallest vibrations or other effects (mechanical play, electromagnetic interference). The ADQ-330/340 series can detect errors by evaluating two consecutive pulses and generate an interrupt if necessary.

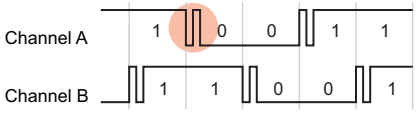


Figure 48: Bouncing of the incremental encoder

Assuming B is set to 1 and A bounces when toggling from 1 to 0, false pulses can be prevented with the following strategy:

- A_{OLD} and B_{OLD} should be the stored values prior a new edge.
- On the first change from A to 0, $A_{OLD} = 0$ and $B_{OLD} = 1$ are stored.
- If now A changes back to 1, no pulse is counted because the current $B = B_{OLD}$.
- As long as B has not changed, edges at A must not be counted.

The logic therefore uses the knowledge that after a change from A, a change from B has to come next (and vice versa). This also applies to reverse direction. If the incremental encoder is driven by a mechanical system with vibrations, for example, these are superimposed on the (rotary) movement and can cause false pulses similar to electric bouncing.

The following state table shows how errors are suppressed by multiple pulses:

A_{OLD}/B_{OLD} → A_{NEW}/B_{NEW}	Direction	Counting	Error (Interrupt)
00 → 00	up	no	no
00 → 01	down	yes	no
00 → 10	up	yes	no
00 → 11	up	no	yes
01 → 00	up	yes	no
01 → 01	up	no	no
01 → 10	up	no	yes
01 → 11	down	yes	no
10 → 00	down	yes	no
10 → 01	up	no	yes
10 → 10	up	no	no
10 → 11	up	yes	no
11 → 00	up	no	yes
11 → 01	up	yes	no
11 → 10	down	yes	no
11 → 11	up	no	no

Legend: Up counting, Down counting, no change of the state, disallowed transition (error).

Figure 49: State table quadrature encoder

Note: The pulse frequency of the incremental encoder must be max. 33 MHz.

3.7.2.4 Frequency measurement

The ADQ-330/340 series has a frequency measuring input which allows you to measure the frequency of a rectangular signal up to about 660 kHz and its duty factor. Each individual measurement must be started by software.

The frequency measuring input FRQ_IN is available on the HDMI connector ST3, pin 9.

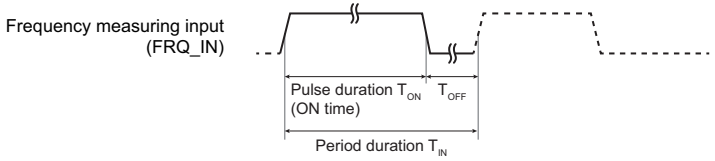


Figure 50: Period and duty factor of a rectangular signal

The frequency measurement range is from f_{IN} = 0.0153 Hz (T_{IN} = 65 s) to f_{IN} = 660 kHz (T_{IN} = 1.5 µs). The period duration of the signal can be resolved in steps of 15.15 ns. Note that the frequency is reciprocally proportional to the period duration. It applies:

$$f_{IN} = \frac{1}{T_{IN}} \qquad T_{IN} = \frac{1}{f_{IN}}$$

The following curve shows that low frequencies can be resolved more accurately than high frequencies:

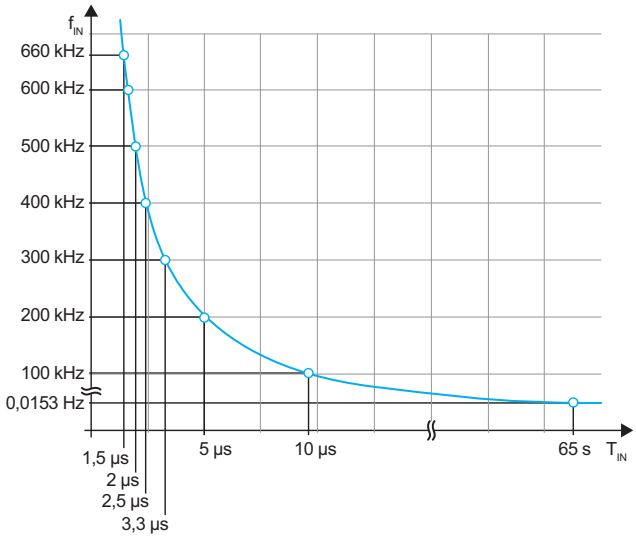


Figure 51: Dependency of frequency from period

In order to calculate the so-called duty factor, the API returns not only the frequency but also the pulse duration (high level) in steps of 15.15 ns. The measurement always starts with the first positive edge of the measuring signal. This means that the duration of the high level is always determined first and returned by the API as T_{ON} time. The duty factor is calculated as follows:

$$\frac{T_{ON}}{T_{IN}} \times 100\% = T_{ON} \times f_{IN} \times 100\%$$

Note: The system-induced measurement error can be up to ±15.15 ns.

The frequency measurement can be reset by software.

3.7.2.5 PWM output

The ADQ-330/340 series provides a PWM output to generate a rectangular signal with adjustable pulse/pause ratio. The frequency f_{OUT} can be set in steps of 15.15 ns in the range between 0.0153 Hz (T_{OUT} = 65 s) and 33 MHz (T_{OUT} = 30 ns). The pulse duration (standard: high level) is given as T_{ON} time in steps of 15.15 ns. The maximum T_{ON} time depends on the selected period T_{OUT}, it is valid: $T_{ONmax} = T_{OUT}$ - 15.15 ns.

The following signals are available on the HDMI connector ST3:

- **Enable input** (PWM_EN, pin 13): High level enables the output operation
- **PWM output** (PWM_OUT, pin 1): Rectangular signal with adjustable duty factor (invertible by software)

The following figure shows a rectangular signal with adjustable duty factor. The duty factor defines the ratio of pulse duration to period duration. In the API, you pass the period duration as frequency ($1/T_{OUT}$) and the pulse duration in seconds. The output must be enabled with a high level at the enable input (PWM_EN) and always starts with the T_{ON} time (high level if not inverted).

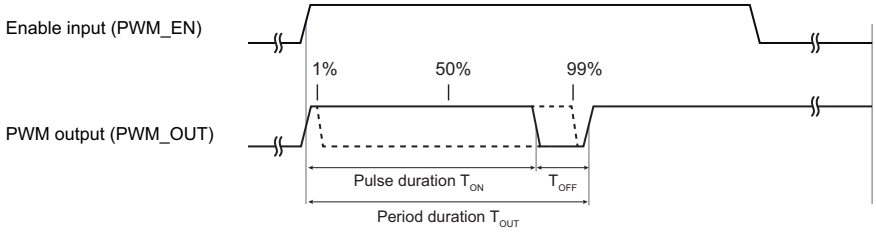


Figure 52: PWM output

The period duration and pulse duration can be resolved in steps of 15.15 ns. Note that the frequency is reciprocally proportional to the period duration. It applies:

$$f_{OUT} = \frac{1}{T_{OUT}} \qquad T_{OUT} = \frac{1}{f_{OUT}}$$

As you can see in Figure 51, slow frequencies can be resolved much accurately than high frequencies. The API automatically sets the next possible value to the desired frequency and returns it.

As soon as low level is applied to the enable input, the output stops. The current configuration and the output level remain unchanged. The configuration is reset by software and the output goes to low level.

3.7.3 Programming

Each functional unit (port) is addressed in the software via a module index.

Please note the order of operation as described in the online help.

4. Appendix

4.1 Specifications

Conditions: T_A = 25°C if not otherwise specified; warm-up time: 30 minutes.
In line with continuous tests we monitor the long-term stability of the specifications regularly.

Analog inputs

Element	Condition	Specification
Channels	ADQ-331/332 ADQ-341/342	16 pseudo differential (2 channel groups)
	ADQ-334/344	32 pseudo differential (4 channel groups)
A/D converter	per channel group	8 channel 18 bit A/D converter with sample & hold stage
Input ranges	Range 0	-10.24 V..(+10.24 V-1 LSB)
	Range 1	0 V..(+10.24 V-1 LSB)
	Range 2	-5.12 V..(+5.12 V-1 LSB)
	Range 3	0 V..(+5.12 V-1 LSB)
Resolution	±10.24 V	1 LSB = 78.1 µV
	0..10.24 V	1 LSB = 39.0 µV
	±5.12 V	1 LSB = 39.0 µV
	0..5.12 V	1 LSB = 19.5 µV
Sample rate (dependent from number of active channels per channel group)	1 channel	800 kS/s
	2 channel	550 kS/s
	3 channel	425 kS/s
	4 channel	350 kS/s
	5 channel	300 kS/s
	6 channel	250 kS/s
	7 channel	225 kS/s
	8 channel	200 kS/s
Bandwidth (-3 dB)		96 kHz
Maximum voltage	Absolute value	19 V_{PP} max.
Total accuracy	±10.24 V	±0.0146%
	0..10.24 V	±0.0126%
	±5.12 V	±0.018%
	0..5.12 V	±0.017%
Integral linearity error	±10.24 V	min. -3.5 LSB, typ. ±1 LSB, max. 3.5 LSB
	0..10.24 V	min. -4 LSB, typ. ±1.5 LSB, max. 4 LSB
	±5.12 V	min. -4 LSB, typ. ±0.75 LSB, max. 4 LSB
	0..5.12 V	min. -6 LSB, typ. ±0.75 LSB, max. 6 LSB

Element	Condition	Specification
Differential linearity error		min. -0.9 LSB, typ. ±0.2 LSB, max. 0.9 LSB
Zero-point error		min. -700 µV, typ. ±160 µV, max. 700 µV
Zero-point error drift		±4 µV/°C
Error on full scale	(FS = full scale)	min. -0.1 %FS, typ. ±0.025 %FS, max. 0.1 %FS
Common mode rejection ratio	CMRR	min. 100 dB, typ. 128 dB
Crosstalk	200 Hz sine in the range ±10.24 V	-109 dB (channel-to-channel without cable at the VHDCI connectors)
Signal noise ratio (SNR)	±10.24 V, f = 2 kHz	min. 93.4 dB, typ. 96.4 dB
	0..10.24 V, f = 2 kHz	min. 87.4 dB, typ. 90.4 dB
	±5.12 V, f = 2 kHz	min. 89.5 dB, typ. 92.5 dB
	0..5.12 V, f = 2 kHz	min. 83.7 dB, typ. 86.6 dB
Total Harmonic Distortion (THD)	±10.24 V, f = 2 kHz	typ. -111 dB, max. -101 dB
	0..10.24 V, f = 2 kHz	typ. -107 dB, max. -99 dB
	±5.12 V, f = 2 kHz	typ. -113 dB, max. -102 dB
	0..5.12 V, f = 2 kHz	typ. -113 dB, max. -100 dB
Input impedance		100 MΩ || 680 pF
Channel list	Channel selection/ range	8 entries per AI module
Timer resolution		in steps of $15.\overline{15}$ ns
Sample time range		1 µs to ~65 s (depending on number of channels)
Trigger modes	Start	Software, digital trigger input per channel group
	Stop	Software, digital trigger input per channel group
Ext. trigger edges		rising, falling, any
Temperature drift		10 ppm/°C
Isolation voltage	ADQ-331/332/334	–
	ADQ-341/342/344	1500 VDC (60 s), A/D section to PC ground
Ground reference	ADQ-331/332/334	GND_PC
	ADQ-341/342/344	GND_AI

Trigger inputs for AI section

Element	Condition	Specification
Number	ADQ-331/332 ADQ-341/342	2 external trigger inputs (one per channel group)
	ADQ-334/344	4 external trigger inputs (one per channel group)
Level max.		-0.5..+5.5 V (different input level on request)
Input level U_{IH}	VCC = 5V	min. 2.2 V
U_{IL}	VCC = 5V	max. 0.8 V
Input current I_F		typ. ±1.6 mA
Trigger clock	Rectangular, symmetrical	max. sample rate of the board
Trigger edges		rising, falling, any
Delay time		max. 30.30 ns
Isolation voltage	ADQ-331/332/334	–
	ADQ-341/342/344	500 VAC to PC ground
Ground reference	ADQ-331/332/334	GND_PC
	ADQ-341/342/344	TRIG_AI_GND

Analog outputs

Element	Condition	Specification
Channels	ADQ-331/341	–
	ADQ-332/342	2 differential voltage outputs
	ADQ-334/344	4 differential voltage outputs
Signal curves		arbitrary, for periodic signals 5 points per period recommended, rectangular signal up to 250 kHz
Resolution		16 bit (1 LSB = 313 µV)
Output voltage range		-10.24 V..(+10.24 V - 1 LSB)
Output current		±10 mA per channel
Capacitive load		max. 1 nF
Total Harmonic Distortion (THD)		at 10 V_{PP}, f = 100 kHz (sine): -96 dB
Transfer rate in steaming operation	PC -> board	max. 25 MHz (cPCI) resp. 30 MHz (PCIe) system dependent*
Output rate max.		500 kS/s (synchronous)
Sample time range		2 µs to ~65 s
Timer resolution		in steps of $15.\overline{15}$ ns
Settling time		0.9 µs
Trigger modes	Start	Software, digital trigger input
	Stop	Software, digital trigger input

Element	Condition	Specification
Ext. trigger edges		rising, falling, any
Total accuracy		±0.01% (±1 mV) from full-scale
Temperature drift		20 ppm/°C
Isolation voltage	ADQ-331/332/334	–
	ADQ-341/342/344	1500 VDC (60 s), D/A section to PC ground
Ground reference	ADQ-331/332/334	GND_PC
	ADQ-341/342/344	GND_AO

* The actual output rate that can be achieved depends largely on the performance of your computer and the number of installed cards and the number of channels used.

Trigger inputs for AO section

Element		Condition	Specification
Number		ADQ-331/341	–
		ADQ-332/342	2 external trigger inputs (one per channel)
		ADQ-334/344	4 external trigger inputs (one per channel)
Level max.			-0.5..+5.5 V (different input level on request)
Input level	U_{IH}	VCC = 5V	min. 2.2 V
	U_{IL}	VCC = 5V	max. 0.8 V
Input current	I_F		typ. ±1.6 mA
Trigger clock		Rectangular, symmetrical	max. output rate of the board
Trigger edges			rising, falling, any
Delay time			max. 30.30 ns
Isolation voltage		ADQ-331/332/334	–
		ADQ-341/342/344	500 VAC to PC ground
Ground reference		ADQ-331/332/334	GND_PC
		ADQ-341/342/344	TRIG_AO_GND

Isolated digital inputs

Conditions: V_EXT_DI = 24 V ±5%, T_A = 25°C

Element	Condition	Specification
Number	ADQ-331/332/334	–
	ADQ-341/342/344	1 x 8 bit digital input ports
Type		Isolated digital inputs (uni-directional) with Schmitt trigger characteristic according to IEC 61131-2 (type 1)

Element	Condition	Specification
Overload protection	on too low ext. supply	Shutdown min. 8.0 V; startup max. 9.6 V; hysteresis typ. 1 V
	on missing ext. supply	Switch-on threshold min. 12.1 V; switch-off threshold max. 13.9 V
Input level	V_EXT_DI = 24 V	L→H: > 15 V; H→L: < 11 V; hysteresis: typ. 1 V
Input current	V_EXT_DI = 24 V	min. 2.3 mA per channel
Status LEDs		per channel
Input filter (programmable per Port)	Filter off (bypass)	typ. 10 µs (N = 1)
	Filter time 1	typ. 1 ms (N = 125)
	Filter time 2	typ. 3.2 ms (N = 400)
	Filter time 3	typ. 10 ms (N = 1248)
Scan frequency	for filters	typ. 100 kHz
Operation modes	Single	Reading single values
	Streaming	max. 10 kHz
	Interrupt	Monitoring the digital ports on bit change or bitpattern match
Externe Versorgung	V_EXT_DI	15..35 VDC, typ. 24 VDC for control engineering
Isolation voltage		500 VAC according to EN60664-1 resp. UL1577
Ground reference		GND_DI (isolated from PC ground GND_PC)

Isolated digital outputs

Conditions: V_EXT_DO = 15…30 VDC, T_A = -25…+125°C

Element	Condition	Specification
Number	ADQ-331/332/334	–
	ADQ-341/342/344	1 x 8 bit digital output ports
Type		Isolated digital outputs (uni-directional) according to IEC 61131-2 (type 1)
Output level	U_{OH}	11..35 V
Output current	U_O = typ. 24 VDC	I_O max. 0.6 A per channel (switching in parallel possibly)
DC short-circuit current	V_EXT_DO = 24 VDC R_L = 10 mΩ	min. 0.7 A; max. 1.7 A
Low voltage shutdown	V_EXT_DO	min. 7 V/max. 10.5 V, restart at max. 11 V, hysteresis: typ. 0.5 V
Over-voltage protection	V_EXT_DO	min. 47 VDC
Discharge energy at inductive load	per channel	max. 1 Joule
Resistance on active output	I_O = 0.5 A; T_A = 25°C	typ. 150 mΩ, max. 200 mΩ

Element	Condition	Specification
Leckage current on deactivated channel		typ. 5 µA, max. 30 µA
Shutdown current on inductive loads		typ. 1.4 A
t_{on} (switch-on time)	R_L = 47Ω, to 90% U_O	typ. 64 µs; max. 120 µs
t_{off} (switch-off time)	R_L = 47Ω, to 10% U_O	typ. 89 µs; max. 170 µs
$dU_O/dt_{(on)}$ (slope at power-on)	from 10..30% U_O, R_L = 47Ω, V_EXT_DO = 15V	typ. 1 V/µs; max. 2 V/µs
$dU_O/dt_{(off)}$ (slope at power-off)	from 70..40% U_O, R_L = 47Ω, V_EXT_DO = 15V	typ. 1 V/µs; max. 2 V/µs
Shutdown temperature		min. 135 °C
Thermal hysteresis		10°K
Operation modes		Simple output, streaming operation
Monitoring	per port	IRQ on thermal overload
Streaming operation	per port	max. 10 kHz
External power supply	V_EXT_DO	11..35 VDC; typ. 24 VDC for control engineering
Isolation voltage		500 VAC according to UL508 & EN 61131-2
Ground reference		GND_DO (isolated from PC ground GND_PC)

Bi-directional digital I/Os (TTL)

Element		Condition	Specification
Number		ADQ-331/332/334	4 x 8 bit port bi-directional
		ADQ-341/342/344	2 x 8 bit port bi-directional
Type			TTL (bi-directional, direction configurable for each 8 bit port)
Level setting			+3.3 V/5 V (switchable by software for all ports together)
Input level	**U_{IH}**	VCC = 5V	min. 2.0 V
	U_{IL}	VCC = 5V	max. 0.8 V
Input current	**I_I**		typ. ±1 µA
Output level	**U_{OH}**	I_O = -24 mA	min. 2.4 V
	U_{OL}	I_O = 24 mA	max. 0.5 V
Output current	**I_O**	je Pin	±24 mA
Operation modes		Single	Read/write of single values
		Streaming	max. 10 kHz
		Interrupt	Monitoring the digital ports on bit change or bitpattern match (not available for ADQ-334 and ADQ-344)
Ground reference			PC ground (GND_PC)

Counter

The specification of the electrical parameters corresponds to those of the bidirectional TTL digital I/Os (see page 62).

Element	Condition	Specification
Counter type		32 bit downward counter
Preset		32 bit start value can be loaded
Mode		Einmaliges Zählen bis Null (retriggerbar) oder kontinuierlich mit automatischem Nachladen des Startwertes
Threshold value	Threshold < Preset	Programmable threshold value, which can trigger an interrupt if the current counter reading is met
Strobe	Strobe < Preset	Pulse duration adjustable in steps of 15.15 ns
Interrupt		On zero crossing or when the threshold value is met
Inputs	via HDMI (ST3)	Enable input (CNT_EN) External trigger input (CNT_TRIG) External clock input (CNT_EXT_CLK)
Output	via HDMI (ST3)	Strobe output (CNT_OUT)

I^2C bus port

The specification of the electrical parameters corresponds to those of the bidirectional TTL digital I/Os (see page 62).

Element	Condition	Specification
Modes		Fast Mode (Fm): 0.4 Mbit/s
Bus subscribers		Max. 128 devices in slave mode addressable; ADQ-330/340 is always master!
Pullup resistors		40 kΩ at I2C_SCL and I2C_SDA to VCC_OUT (3.3 V or 5 V, depending on global TTL level setting)
Bus signals	via HDMI (ST3)	Clock line "Serial Clock" (I2C_SCL) Data line "Serial Data" (I2C_SDA)
Address format		7 bit slave address + read/write bit as LSB
Data format		Up to 4 data bytes can be transferred per write or read cycle

Incremental encoder (in preparation, all details without guarantee)

The specification of the electrical parameters corresponds to those of the bidirectional TTL digital I/Os (see page 62).

Element	Condition	Specification
Counter type		16 bit up/down counter + direction of movement
Quadrature signal		A/B channel with 90° phase shifting
Coding		Gray code
Resolution		4-fold per signal period ("each edge counts")
Error correction		Suppression of invalid states on hardware level
Pulse frequency sensor		max. 33 MHz
Reset input		asynchronous reset, sets the counter to 0000 Hex
Interrupt		Interrupt on exceeding the counter range

Element	Condition	Specification
Inputs	via HDMI (ST3)	Sensor input "Channel A" (INC_A) Sensor input "Channel B" (INC_B) External reset input (INC_EXT_RST)

Frequency measurement

The specification of the electrical parameters corresponds to those of the bidirectional TTL digital I/Os (see page 62).

Element	Condition	Specification
Measuring range	Frequency (period)	f_{IN} = 0.0153 Hz (T_{IN} = 65 s) to f_{IN} = 660 kHz (T_{IN} = 1.5 µs).
	Pulse duration (High)	T_{ON} in steps of 15.15 ns
Resolution	Period & pulse	15.15 ns (see also Figure 51 on page 54)
Accuracy	determined by the system	±15.15 ns
Input	via HDMI (ST3)	Frequency measuring input (FRQ_IN)

PWM output

The specification of the electrical parameters corresponds to those of the bidirectional TTL digital I/Os (see page 62).

Element	Condition	Specification
Rectangular signal output	Frequency (period)	f_{OUT} = 0.0153 Hz (T_{OUT} = 65 s) to f_{OUT} = 660 kHz (T_{OUT} = 1.5 µs).
	Pulse duration (High)	T_{ON} in steps of 15.15 ns; T_{ONmax} = T_{OUT} - 15.15 ns
Duty factor	Pulse duration/period	Duty factor (T_{ON}/T_{OUT}) can be calculated by the values returned by the function `adqPWMConfig()`
Resolution	Period & pulse	15.15 ns (see also Figure 51 on page 54)
Input	via HDMI (ST3)	Enable input (PWM_EN)
Output	via HDMI (ST3)	PWM output (PWM_OUT), can be inverted by software

General

Element	Condition	Specification
PC interface	cPCI models	CompactPCI bus (32 bit, 33 MHz) Rev. 2.2
Power consumption cPCI models	Idle operation	+3.3 V: 25 mA +12 V: 15 mA
Fuses for external power supply via ST1	5 V (F1)	3 A (self-recovering, type: Polyfuse)
	12 V (F2)	2 A (self-recovering, type: Polyfuse)
Temperature range	Operation	0..70 °C (standard)
	Storage	-40..100 °C
Humidity	Operation	20%..55% (not condensing)
	Storage	5%..90% (not condensing)

Element	Condition	Specification
Physical size (without mounting bracket and connectors)	cPCI models	3 U CompactPCI board, 4 HP wide
Connectors	ST1	3-pol. connector, type: Phoenix Contact MC 1,5/ 3-G-3,5 (grid spacing: 3.5 mm)
	ST2A, ST2B	Two 68-pin VHDCI female connectors
	ST3	HDMI connector, type HEC
	ST4	25-pin D-Sub female connector via additional mounting bracket/bezel
	ST5	20-pin IDC connector
Certifications		EMC Directive 2004/108/EG, Emission EN 55022, Noise immunity EN 50082-2, RoHS
Manufacturer warranty		36 month

4.2 Pinout

4.2.1 68-pin VHDCI female connectors ADQ-33x (ST2A/B)

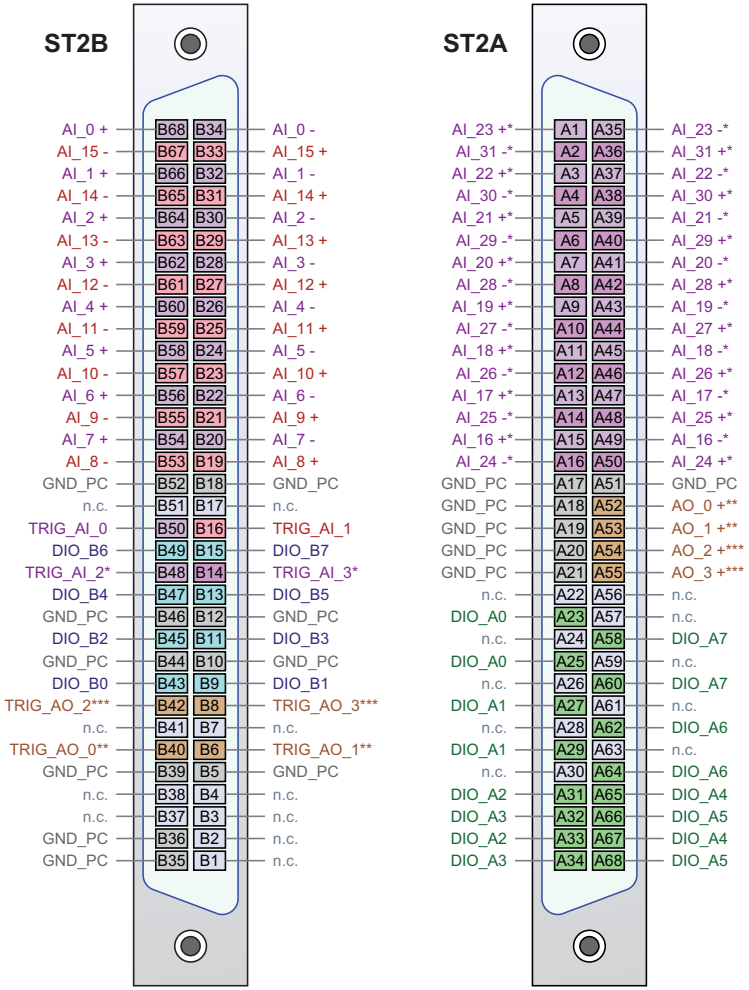


Figure 53: Pinout of the 68-pin VHDCI female connectors for ADQ-33x (ST2A/B)

Note: The digital I/Os DIO_A0..7 are each routed to two pins.

* Analog inputs only available on ADQ-334. Else not connected.
** Analog outputs only available on ADQ-332 and ADQ-334. Else not connected.
*** Analog outputs only available on ADQ-334. Else not connected.

4.2.2 68-pin VHDCI female connectors ADQ-34x (ST2A/B)

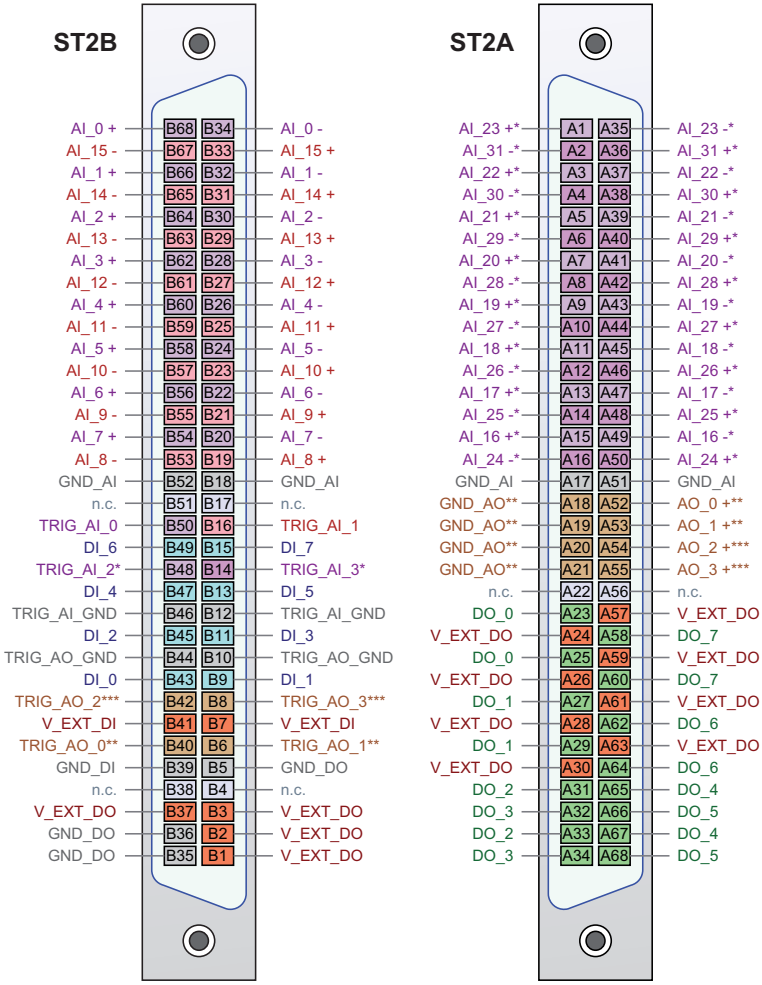


Figure 54: Pinout of the 68-pin VHDCI female connectors for ADQ-34x (ST2A/B)

Note: To use the maximum current of up to 0,6 A per digital output DO_0..7, the external power supply should be connected with all the 8 pins of V_EXT_DO. Correspondingly the outputs DO_0..7 should be each connected via two pins.

* Analog inputs only available on ADQ-344. Else not connected.
** Analog outputs only available on ADQ-342 and ADQ-344. Else not connected.
*** Analog outputs only available on ADQ-344. Else not connected.

4.2.3 HDMI connector (ST3)

HDMI connector type HEC for the following special functions:

- Counter (prefix: CNT…)
- I²C-bus port (prefix: I2C…)
- Incremental encoder port (prefix: INC…)
- Frequency measurement input (prefix: FRQ…)
- PWM output (prefix: PWM…)

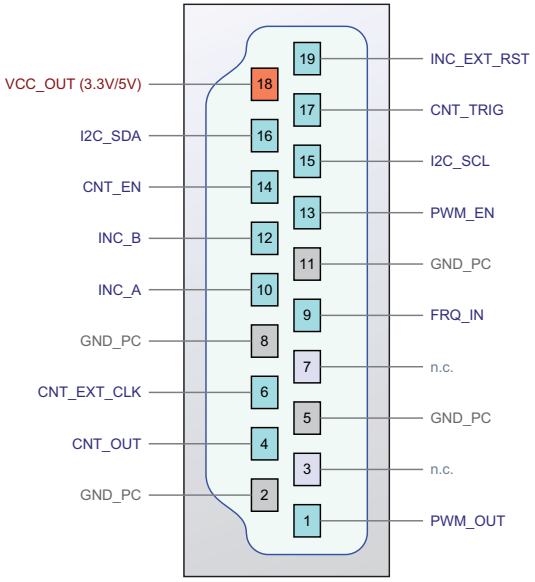


Figure 55: HDMI connector for special functions (ST3)

4.2.4 Supply connector for field wiring (ST1)

3-pin connector, type Phoenix Contact MC 1,5/ 3-G-3,5 (grid spacing: 3.5 mm).

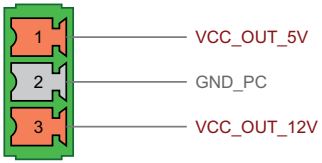


Figure 56: Power supply connector for field wiring (ST1)

4.2.5 25-pin D-Sub female connector (ST4)

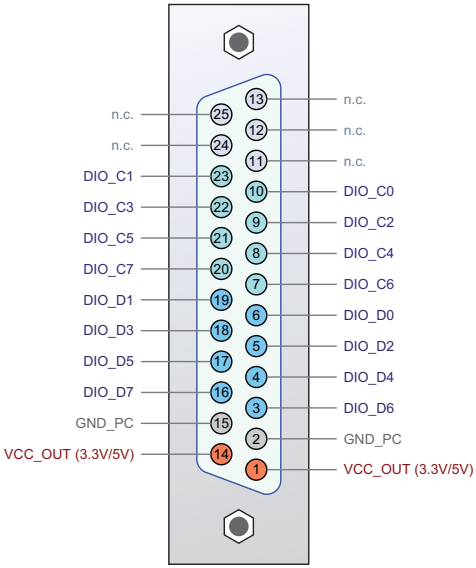


Figure 57: Pinout 25-pin D-Sub female connector (ST4)

4.2.6 Adapter cable with additional front bezel/mounting bracket

To use the TTL digital I/Os (port DIO_Cx and DIO_Dx) you need an adapter cable with additional front bezel/mounting bracket (included) from the 20-pin IDC connector ST5 of the board to the 25-pin D-Sub female connector ST4.

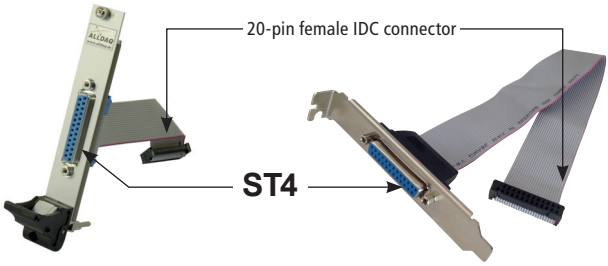


Figure 58: Additional front bezel/mounting bracket

Connection of the flat-ribbon cable to ST5

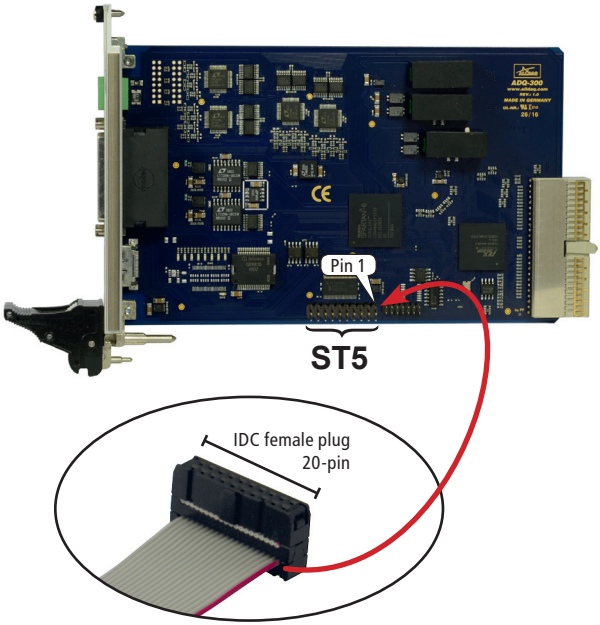


Abb. 59: Connection of flat-ribbon cable to ST5

Note: When connecting the adapter cable, connect pin 1 of the flat-ribbon cable (red marked cable) to pin 1 of the IDC male connector ST5 as shown above.

Pin ST5	Description	Pin ST5	Description
1	VCC_OUT (+3,3 V/5 V)	11	DIO_D0
2	VCC_OUT (+3,3 V/5 V)	12	DIO_D1
3	GND_PC	13	DIO_C6
4	GND_PC	14	DIO_C7
5	DIO_D6	15	DIO_C4
6	DIO_D7	16	DIO_C5
7	DIO_D4	17	DIO_C2
8	DIO_D5	18	DIO_C3
9	DIO_D2	19	DIO_C0
10	DIO_D3	20	DIO_C1

Table 9: Pinout ST5

4.2.7 Special terminal block

Special terminal block for ADQ-330/340 series. The connection to the board is made by two 68-pin VHDCI and a HDMI cable.

The signals are provided via 14 x 10-pin clamps of type Phoenix Contact MCV 1,5/10-G-3,81. The corresponding mating plug with push-in spring connection of type Phoenix Contact FMC 1,5/10-ST-3,81 (grid spacing: 3.81 mm) are included with the terminal block.

Additionally 8 analog inputs and 4 analog outputs can be attached by BNC female connectors.

The imprint of the terminal block shows the pin assignment.

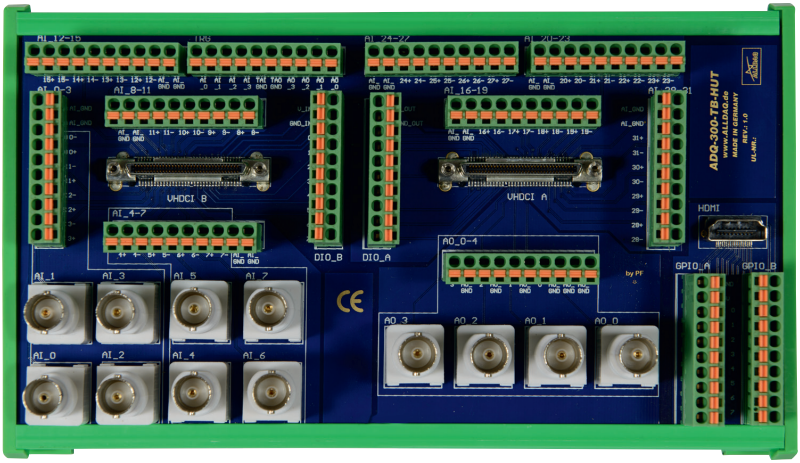


Figure 60: Special terminal block for ADQ-330/340 series

4.3 Accessories

4.3.1 Terminal blocks

- **ADQ-TB-300-HUT** (Art. no. 146811)
  Special terminal block for ADQ-330/340 series for mounting on DIN rail. The connection to the board is made via two 68-pin VHDCI and one HDMI connectors. The signals are provided by 14 x 10-pin Phoenix type clamps. Additionally 8 analog inputs and 4 analog outputs are provided by BNC female connectors.
- **ADQ-TB-D25M-HUT** (Art. no. 111749)
  25-pin connector block for mounting on DIN rail, 25-pin D-Sub male connector to Phoenix typ clamps.

4.3.2 Cables

- **ADQ-CR-VHDCI-68M/68M-0,9m** (Art. no. 146812)
  Double-shielded round cable from 68-pin VHDCI male connector to 68-pin VHDCI male connector, twisted pair lines, length: ca. 0.9 m
- **ADQ-CR-VHDCI-68M/68M-1,8m** (Art. no. 146813)
  Double-shielded round cable from 68-pin VHDCI male connector to 68-pin VHDCI male connector, twisted pair lines, length: ca. 1.8 m
- **ADQ-CR-HDMI-MM-1m** (Art. no. 127015)
  HDMI cable for connection of the digital I/O and trigger lines with the special terminal block, length: ca. 1 m
- **ADQ-CR-D25M-D25F-1,8m** (Art. no. 111752)
  Shielded round cable from 25-pin D-Sub male connector to 25-pin D-Sub female connector, length: 1.8 m

4.3.3 Additional front bezel/mounting bracket

- **ADQ-AP-D25F-cPCI** (Art. no. 111755 - included with ADQ-330/340 cPCI models)
  CompactPCI bezel (4HP) with 25-pin D-Sub female connector to 20-pin IDC female connector
- **ADQ-AP-D25F-PCI** (Art. no. 111756 - included with ADQ-330/340 PCIe models)
  PCI mounting bracket with 25-pin D-Sub female connector to 20-pin IDC female connector

4.4 Manufacturer and support

ALLNET® and ALLDAQ® are registered trademarks of the ALLNET® GmbH Computersysteme. For questions, problems and product information please contact the manufacturer directly:

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4.5 Important notes

4.5.1 Packaging ordinance

Basically manufacturer and distributors are committed to take care, that sales packaging are withdrawn after use from the end user and applied to a new disposal or to a material recycling as a matter of principle (translated according to § 4 sentence 1 of VerpackVO). If you have problems as customer on disposal of packaging and shipping material please write an email to info@allnet.de.

4.5.2 Recycling note and RoHS compliance

Please note, that parts of products of ALLNET® GmbH should be disposed in recycling centers resp. may not be disposed via the household waste (printed circuit boards, power adapters and so on).

ALLNET® products are manufactured in accordance with RoHS (RoHS = Restriction of the use of certain hazardous substances).

4.5.3 CE certification

The ADQ-330/340 series is CE certified.

This device is compliant to the EU directive: 2004/108/EG regarding the electromagnetic compatibility (EMC) and the cross approval of their conformity. The conformity with the directive as stated above is confirmed by the CE sign on the device.

4.5.4 Warranty

Within the warranty time we eliminate manufacturing and material defects free of charge. The warranty terms valid for your country can be found on the homepage of your distributor. If you have questions or problems applying the warranty you can contact us during our normal opening hours under the following phone number +49 (0)89 894 222 – 474 or by email: support@alldaq.com.

5. Index

S

T

V

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ALLDAQ

Competence in Measurement

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